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Utpal Kalita, Christian Tückmantel, Thomas Riedl, Ullrich R. Pfeiffer

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Evaluation of the Beyond-f_T Operation of an IGZO TFT-Based RF Self-Mixing Circuit

U. Kalita, C. Tueckmantel, T. Riedl, U. Pfeiffer, *Senior Member, IEEE*

***Abstract*—The objective of this study is to show the potential of amorphous indium gallium zinc oxide (a-IGZO) thin film transistors (TFT) for designing RF communication systems operating in the GHz regime. For that purpose, the self-mixing operation of in-house fabricated IGZO-TFTs beyond their transit frequency (f_T) is reported. The bottom-gate, top-contact TFTs have an f_T of 40 MHz including the device interconnects. A differential RF self-mixing circuit was fabricated to act as an RF detector and frequency doubler. The detector shows a peak voltage responsivity (R_V) and a minimum noise equivalent power (NEP) of 445 V/W and 0.1 nW/$\sqrt{\text{Hz}}$ at 50 MHz and 2 V/W and 30 nW/$\sqrt{\text{Hz}}$ at 1 GHz respectively, at a chopping frequency of 28 kHz. As a frequency doubler, the circuit can generate a second harmonic output voltage up to –36 dBV for an 8 dBV RF input voltage at 100 MHz.**

***Index Terms*—transit frequency (f_T), amorphous indium gallium zinc oxide (a-IGZO), thin film transitor (TFT), self-mixing, responsivity (R_V), noise equivalent power (NEP).**

I. Introduction

METAL-OXIDE thin-film transistors (TFTs) have been intensively studied over the past 15 years [1], [2], [3]. More recently, the scope of applications for metal-oxide TFTs has been widened and includes radio-frequency (RF) communication systems [4]. Compared to state-of-the art crystalline silicon MOSFETs, amorphous metal-oxide TFTs still demonstrate comparatively low f_T. Specifically, TFTs based on IGZO have been reported with an f_T of 135 MHz on a flexible substrate [5]. More recently, in ZnO-based TFTs, the highest f_T of 860 MHz has been achieved using techniques that are compatible with large-area applications on flexible substrates [6]. However, the 1 GHz f_T barrier has not been overcome on the device level so far. For designing RF communication building blocks based on metal-oxide TFTs operating in the GHz frequency range, innovative harmonic circuits that operate beyond-f_T are required. The concept of a square-law power detector circuit using resistive self-mixing in a differential CMOS topology has been proposed for terahertz wave detection in [7]. In this paper, we explore this circuit concept for metal-oxide TFTs to detect RF signals in the range of 50 MHz to 2 GHz. We further describe the performance of the same circuit as a frequency doubler for a 100 MHz RF input signal.

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U. Kalita and U. Pfeiffer are with the Institute of High-Frequency and Communications Technology (IHCT), University of Wuppertal, Wuppertal, Germany (e-mail: kalita@uni-wuppertal.de, ullrich.pfeiffer@uni-wuppertal.de).

C. Tueckmantel and T. Riedl are with the Institute of Electronic Devices, University of Wuppertal, Wuppertal, Germany (e-mail: c.tueckmantel@uni-wuppertal.de, t.riedl@uni-wuppertal.de)

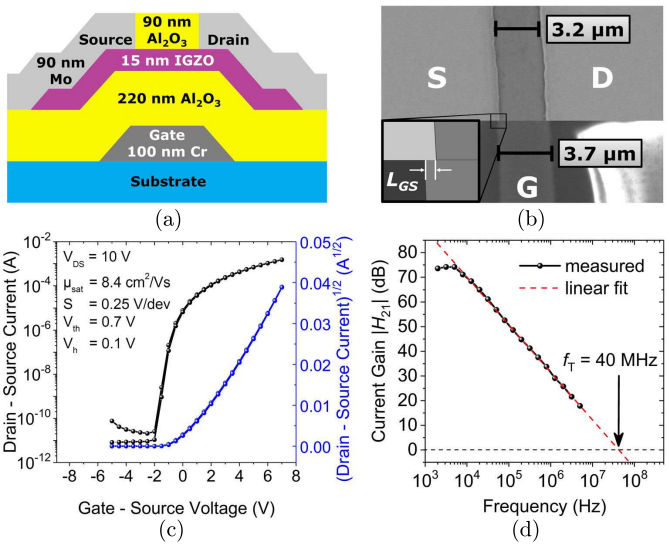

Fig. 1. (a) Schematic of the TFT cross-section, (b) SEM image and a magnified sketch of the parasitic overlap L_{GS} between gate and source electrodes; overall overlap $L_{ov} = L_{GS} + L_{GD}$ = 0.5 µm for a TFT with channel length L of 3.2 µm, (c) current-voltage transfer characteristics and (d) current gain $|H_{21}|$ with extrapolated f_T of 40 MHz of the TFT.

II. Fabrication and Characterization of Transistors

A cross-section of the TFT layout with the respective layer thicknesses can be found in Fig. 1(a). To limit the parasitic overlap capacitances between the source/drain (S/D) electrodes and the gate electrode, we implemented a self-aligned photolithography process for patterning of the S/D electrodes in a staggered bottom-gate configuration. Gate electrodes made of Cr were deposited by sputtering and patterned by photolithography on a glass substrate. Next, a gate dielectric of 220 nm Al_2O_3 was formed on top using atomic layer deposition (ALD). Subsequently, a 15 nm thick a-IGZO layer was deposited by RF magnetron sputtering at room temperature through a metal shadow mask. Sputtering was done in Ar atmosphere with 0.8% O_2 content and chamber working pressure of 6.6 mTorr at a plasma power of 125 W using a ceramic $InGaZnO_4$ (In:Ga:Zn = 1:1:1 atomic %) target. After that, a post-deposition heat treatment at 350°C in vacuum was performed. The predefined gate electrodes were then used as a shadow mask for lithographic lift-off structuring of the S/D electrodes. To prepare the self-aligned S/D electrodes, a

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thermally evaporated 90 nm thick layer of Molybdenum (Mo) was used due to its brittleness, adhesiveness to oxide and sharp edges. A 3.7 µm wide gate electrode finally resulted in a S/D distance (channel length) of 3.2 µm and a parasitic overlap of 500 nm. A sketch of the gate-source overlap L_{GS} is drawn in the inset of Fig. 1(b) for better clarity. The fabrication process of the TFTs was finalized by a deposition of 90 nm thick ALD-grown Al_2O_3 back channel encapsulation layer using Ozone as oxidant [8].

Fig. 1(c) shows an exemplary transfer characteristic of the fabricated 500/3.2 µm/µm IGZO TFT measured under ambient conditions. This is the representative device among the twelve overall devices that were characterized. A saturation field effect mobility μ_{sat} of 8.4 cm^2/Vs and a threshold voltage V_{th} of around 0.7 V can be extracted from the transfer characteristics, measured at drain-source bias V_{DS} of 10 V. At this bias point, it is ensured that the TFT operates in the saturation regime for all swept values of gate-source voltage V_{GS}. Therefore, bias points of V_{GS} = 7 V, V_{DS} = 10 V have been selected for the following AC characterization.

The transistor f_T has been derived from measured Y-parameters. A Solartron 1260A Impedance/Gain-Phase analyzer was connected to the gate and the drain of the TFT, which supplied an AC signal of 100 mV peak-to-peak voltage amplitude, as well as a DC bias voltage to the gate. A Keithley 237 SMU supplied the DC bias voltage V_{DS}, while the source contact of the TFT was grounded. First, the short-circuit input admittance Y_{11} (at V_{DS} = 0 V) was measured followed by short-circuit forward-transfer admittance Y_{21} (at V_{DS} = 10 V) measurement in the frequency range of 2 kHz to 5 MHz. Finally, the current gain H_{21} was calculated from $H_{21} = Y_{21}/Y_{11}$. Fig. 1(d) shows the absolute value of the calculated H_{21} of our IGZO TFT. By extrapolation of the $|H_{21}|$ to unity, an f_T of 40 MHz has been determined. The extracted value matches the theoretical one for a 3 µm long TFT with a parasitic overlap of 500 nm [9].

III. Device Operation Beyond f_T

A photograph of the fabricated electronic power detector is shown in Fig 2(a).

The square-law power detector works on the principle of resistive self-mixing of the applied AC signal. At frequencies below f_T, the self-mixing can be explained by quasi-static model as depicted in Fig. 2(b). In this case, the self-mixing of the RF signal occurs due to the shared virtual AC-ground between the gate and the drain [10]. From [7], the square-law relation between the total drain current i_{ds} and an applied RF signal v_{RF} in strong inversion of the channel can be expressed as

$$i_{ds}(t) = \frac{W}{L}\mu C_{ox}(v_{RF}(t)^2/2 + v_{RF}(t)(V_G - V_{th})), \quad (1)$$

where W and L are the width and length of the channel, μ is the carrier mobility, C_{ox} is oxide capacitance per unit area, V_G is the gate-bias voltage and V_{th} is the threshold voltage. Considering v_{RF} to be a time harmonic AC-signal $v_{RF} = V_{RF}cos(\omega t)$, the current can be formulated from (1) as

$$i_{ds}(t) = \mu C_{ox}\frac{W}{4L}V_{RF}^2(1 + cos(2\omega t)). \quad (2)$$

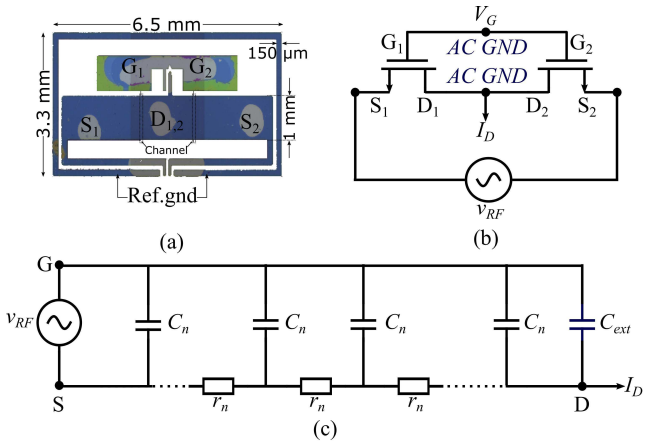

Fig. 2. (a) An image of the differential detector, (b) the quasi-static model of the detector and (c) RC ladder network model of a transistor channel.

The first term in the right-hand side of (2) corresponds to the DC current used for detection, whereas the second term generates the second harmonic component necessary for frequency doubling. The odd harmonics would cancel out due to the differential architecture. The current through the output resistance of the transistor would create an output voltage that can be measured with a spectrum analyzer.

For frequencies above the device f_T, the non-quasi-static model is applied. Here, each channel is modeled as an RC-ladder [7] shown in Fig. 2(c). C_{ext} represents the shared AC ground at low frequency. The channel is divided into n segments, where each segment is equipped with a gate-to-channel voltage dependent resistance r_n and a segment capacitance C_n. The gate-to-channel voltage $v(x,t)$ depends on both time t and distance x in the channel from the source v_{RF}. For strong inversion of the channel, in the linear region of the transistor, C_n and r_n are related as $1/r_n = \mu C_{\mathrm{n}}(v(x,t) - V_{th})$. This leads to a partial differential equation for time and space derivatives as

$$\frac{\partial v(x,t)}{\partial t} = \frac{\partial}{\partial x}[\mu(v(x,t) - V_{th})\frac{\partial v(x,t)}{\partial x}]. \quad (3)$$

A numerical approach to solve the above equation and to obtain the distributive resistive self-mixing has been presented in [7]. This principle enables the differential architecture to function as a detector.

IV. Measurements and Results

The measurement setup for the detector is shown in Fig. 3. For its linear operation as a power detector, a –10 dBm RF input signal is applied by a Keysight E8257D synthesizer. The RF signal is chopped at 28 kHz to nullify the effect of the device flicker noise. Nine different radio frequencies between 50 MHz to 2 GHz are selected. A bias tee and a power splitter are used to combine the signal with the DC ground and to create two differential signals respectively. A variable gate bias voltage V_G is provided by a R&S HMP4040 programmable power supply unit. The supply voltage V_{DD} is delivered by a Keithley 2400 source meter unit through a 680 kΩ resistance, in order to prevent loading of the detector output V_{OUT} by the source meter unit. The output of the detector is read using a

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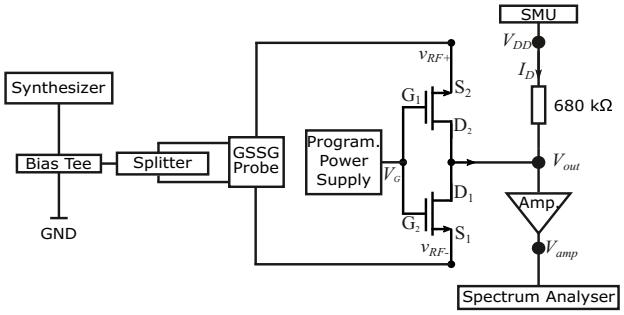

Fig. 3. Measurement setup for the detector.

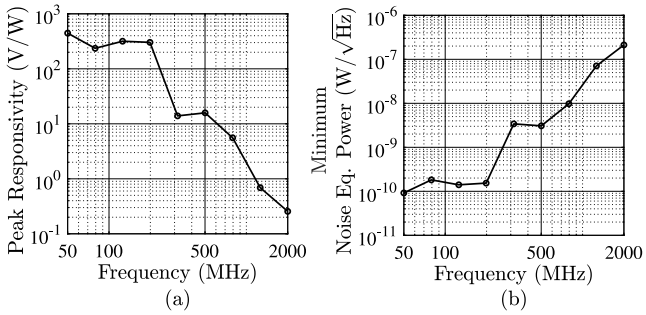

Fig. 4. Measured (a) peak responsivity and (b) minimum noise equivalent power over frequency for the differential detector.

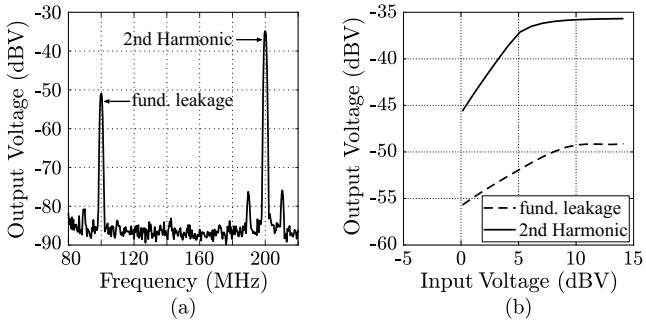

Fig. 5. (a) Output spectrum at compression of the doubler and (b) input vs. output RF voltage characteristic of the differential frequency doubler for the fundamental (100 MHz) leakage and second harmonic (200 MHz) outputs.

DC needle, which in turn is coupled to a FEMTO HVA-10M-60-F amplifier with a voltage amplification of 40 dB, an input impedance of 1 MΩ and an output impedance of 50 Ω. The amplified output voltage is read through an Agilent E4440A spectrum analyzer for different values of V_{DD} and V_G.

The performance of a detector is evaluated by measuring its peak R_V and minimum NEP at bias points corresponding to the maximum signal-to-noise ratio [7]. The R_V of a detector is defined as the ratio between the output voltage V_{OUT} and the input power P_{in} i.e. $R_V = V_{OUT}/P_{in}$. The attenuation in the measurement setup and the reflected power from the circuit are de-embedded from P_{in} using S-parameters measurements. The NEP is then calculated from $NEP = V_N/R_V$, where V_N is the output spot noise voltage calculated per Hz.

The measured peak R_V and minimum NEP are plotted for the nine different frequencies in Fig. 4(a) and 4(b) respectively. These R_V maxima and NEP minima are obtained at different values of V_G for each frequency. The peak R_V is 445 V/W at 50 MHz and decreases to 2 V/W at 1 GHz. The minimum NEP on the other hand is 100 pW/$\sqrt{\text{Hz}}$ at 50 MHz and increases to 30 nW/$\sqrt{\text{Hz}}$ at 1 GHz. The CMOS differential detector consisting of two 0.25 µm long and 0.78 µm wide FETs presented in [7] demonstrated an NEP of 300 pW/$\sqrt{\text{Hz}}$ at 19·f_T, which is one order of magnitude lower than the NEP of our circuit at 19·f_T. At 2 GHz, which is equal to 25·f_T, the signal is still detectable with a R_V of 0.2 V/W and a minimum NEP of 200 nW/$\sqrt{\text{Hz}}$.

In order to measure the performance of the same circuit as a doubler, a pair of 100 MHz differential signals (without chopping) of varying amplitude are applied to its source terminals. The output signal at the drain terminal is measured using a GS probe that is grounded only off-chip. It is then AC-coupled to a FEMTO HVA-200M-40-F voltage amplifier and the spectrum analyzer at the bias point V_D= 4 V, V_G= 2.5 V. The bias point corresponds to the maximum output voltage at the second harmonic, as observed in the spectrum analyzer. The gain of the amplifier is de-embedded from the measured data.

As shown in Fig. 5(a), the output spectrum depicts a fundamental leakage and a second harmonic component at compression. The doubler reaches compression at around 8 dBV of input voltage as shown in Fig. 5(b). At this point, the second harmonic output voltage is –36 dBV. A higher conversion gain is envisaged by design of adequate input and output conjugate matching networks in future. The fundamental leakage output of about -50 dBV at compression is caused by asymmetries between the threshold voltages and the transconductances of the TFTs, which have to be mitigated in future to improve the spectral purity of an output signal.

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