A 32×32 Pixel 0.46-to-0.75THz Light-Field Camera SoC in 0.13µm CMOS

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34.3 A 32×32 Pixel 0.46-to-0.75THz Light-Field Camera SoC in 0.13μm CMOS

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Light-field (LF) refers to the spatio-directional light flow in space. In LF imaging, light rays are recorded along different positions and directions, and a 3-D scene is reconstructed with back-propagation [1]. Modern visible-light LF cameras assemble a lens array atop a megapixel (Mpx) count focal-plane array (FPA), such that each lens (macro-pixel) provides spatial sampling while the FPA pixels within a lens (sub-pixels) provide angular sampling [2]. Likewise, THz LF cameras can allow real-time 3D see-through imaging for inspection and screening applications [3]. Unfortunately, THz Mpx FPAs are infeasible as a large THz pixel area (>10x visible-light pixel) would require wafer-scale FPA fabrication, leading to impractical costs and process variations. Multi-chip packaging is an alternative for scaling the THz FPA pixel count, but it requires compact THz camera ICs with serial data interfaces (small pin count) to allow dense integration.

This paper presents a fully integrated 32×32 pixel THz camera system-on-a-chip (SoC) implemented in a low-cost CMOS process, which combines antenna coupled pixels, programmable readout (RO) gain, signal digitization, and serial data interface in a single monolithic IC. The implemented antenna design allows a compact pixel and die area while maintaining optimal performance at the mid-THz band (0.4–0.7THz) where state-of-the-art (SOTA) high power silicon THz sources are emerging. Attached to a Silicon (Si) lens, the SoC is capable of an optimum angular light-field sampling (approx. -3dB beam overlap) within its field-of-view (FoV) in the mid-THz band. This SoC exhibits the highest integration complexity for any THz camera to date, allowing compact-sized 8-pin (integrated bias) or 16-pin (external bias) die packaging for dense, large pixel count imaging arrays for scalable THz imaging systems including (but not limited to) multi-chip THz LF imager as shown in Fig.1.

The SoC block diagram is shown in Fig.2. The chip is implemented in a 130nm CMOS process with 7-layer BEOL. Each pixel consists an isolated nMOS detector-pair driven differentially with a linearly polarized rectangular wire-loop antenna which is illuminated by the Si-lens through the chip backside (estimated lens-antenna gain = 40dBi per pixel for 15mm Si-lens). For a compact footprint, two additional tapered slots are inserted along the antenna H-plane to extend its operation range toward lower frequencies by increasing the effective length of the current flow path. The serpentine strip feeding the main loop creates a highly inductive input impedance across the antenna operation bandwidth (BW). The 48μm×60μm antenna provides a high-efficiency (>70%) operation from around 500GHz towards 2THz, with an optimum impedance match at around 600–700GHz.

The camera operates on rolling shutter with multiplexed row selection and column parallel RO. A pixel is activated and deactivated by applying optimum gate-bias Vg (0.6V) and supply-bias VDD (1.2V) respectively to the detector nMOS gate. The in-pixel RO circuit converts the THz photo-current response into a voltage (sim. gain 139dBΩ, linearity = -15dBm, dc power consumption Pdc = 5μW) which is fed to a differential cascode stage with column shared active load (sim. gain 7dB, Pdc = 80μW per column). The columns are multiplexed to a shared RO chain integrating a programmable gain amplifier (PGA, sim. gain -16dB to 22dB, Pdc = 480μW), correlated double sampler (CDS), second identical PGA, and a range adjustable 6-bit flash ADC (FADC). All dc biases can be either programmed with an integrated bias generator or applied externally. The analog PGA outputs can also be monitored externally. An integrated ASIC with SPI provides the timing, gain, and bias controls.

The current-mode in-pixel RO scheme is elaborated in Fig.3. The detector nMOS source-drain terminals are interfaced differentially to diode-connected nMOS transistors M1-M2 with active pMOS load M5-M6. The detector nMOS can be modeled as a gate-bias dependent resistance Rch. When optimum bias Vg is applied in presence of a THz signal at the antenna, the photo-current *Iph* is generated parallel to Rch and flows from drain-load (M2) to source-load (M1). This is mirrored to M3-M4 with x32 amplification and is converted to a voltage signal. In conventional voltage-mode RO [4] the amplifier circuit is biased through the detector resistance Rch which is large for optimum THz rectification bias. This creates unwarranted, slow floating offsets which reduce the overall dynamic range (DR). In comparison, our scheme allows well-defined dc bias for the RO circuit irrespective of the bias dependent Rch. The M1-M2 transistors have a high resistance (narrow aspect ratio) to minimize detector shunted photo-current *i'* while maintaining drive voltage for M3-M4. The final sizing of transistors was optimized with large signal harmonic balance simulations. Further optimization is achieved with programmable bias Vpix at M5-M6 gate. Each pixel also integrates individual 5-bit DAC (Fig. 2) to compensate potential M1-M2 mismatch related offsets (±10mV) as these transistors operate in the weak-inversion region. The array exhibits process related pixel-to-pixel variation, including threshold voltage related variation in the detector resistance Rch. Note that detector bias switching also causes charge transients due to parasitic capacitors (Cgd, Cgs, Cp), but these are filtered by the limited BW at M3-M4 amplification stage. At the optimum bias (Vg=0.6V, Vpix=0.81V), the simulated 3dB BW of the in-pixel readout is around 430kHz, which was optimized to provide the largest noise integration period for video-rate imaging. The SoC die area and total measured dc power consumption are 8.5mm^2 and 13.5mW (13mW analog + 500μW digital) respectively. The chip was packaged with a 15mm Si lens into a camera module with an overall power consumption of 153mW (including an FPGA-based USB interface).

The camera performance (Fig.4) was experimentally characterized with two techniques. The video-mode characterization was performed with a continuous-wave (CW) -8dBm, 0.65THz waveguide horn-antenna coupled source in a back-to-back arrangement. Full frame images were recorded at 25fps. A mean pixel responsivity Rv of 171kV/W (sim. gain 141dBΩ) and an integrated minimum pixel NEP of 36nW were observed at the optimum bias. To ascertain the RF BW, a broadband characterization was also performed with a tunable CW THz photo-mixer source (sweep frequency 100GHz-1320GHz, output power -10 to -30dBm) in a chopped (40kHz) collimated beam setup. The response from one central pixel was monitored at the output of the first PGA. Here, the max. Rv and min. NEP were calculated as 35kV/W (sim. gain 128dBΩ) and 262pW/√Hz respectively at 600GHz. A 3dB RF BW of 290GHz (460-750GHz), and a 10dB operational RF BW of 575GHz (415-990GHz) were also measured. In both measurements, the noise-sensitive biases Vpix and Vg were applied externally, also to avoid any process related variation of the internal bias generators.

The LF imaging with angular sampling is demonstrated with vector illumination reconstruction of a 0.65THz source [3]. A virtual 11×11 camera array was synthesized by moving the module with 1.5cm (lens-size) spacing in a plane approx. 20cm away from the source. The LF reconstructed image is shown in Fig.5. No prior knowledge was assumed about the source, yet the LF recreated illumination pattern predicts a Gaussian beam profile and ±4° HPBW (actual ±5.5°). The data was recorded in 35 minutes (100 frames averaging), which can be reduced to less than 17s with a real 11×11 camera array.

The comparison of this work with other SOTA silicon integrated THz cameras is shown in Fig.6, and the die micrograph is shown in Fig.7. Compared to other implementations, our SoC demonstrates a broadband CW (non-chopped) low power THz digital camera system fully integrated within a small die area. The SoC maintains an optimum performance in the more practical mid-THz band. Its low power consumption and small pin count enables large THz LF camera arrays, so that several images can be recorded and synthetic images in combination with computational techniques can be created.

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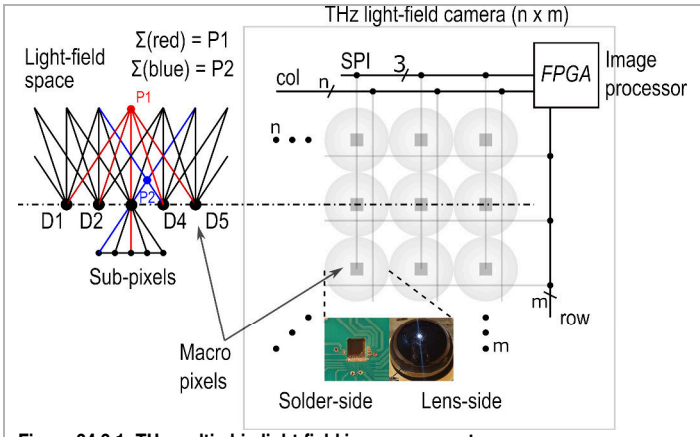

Figure 34.3.1: THz multi-chip light-field imager concept

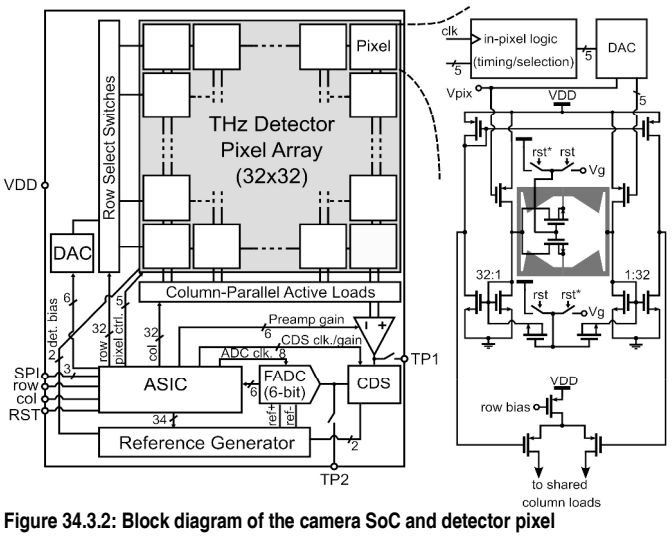

Figure 34.3.2: Block diagram of the camera SoC and detector pixel

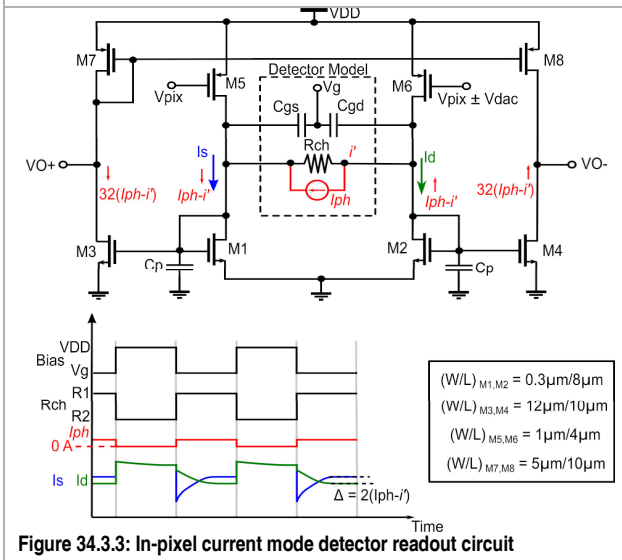

Figure 34.3.3: In-pixel current mode detector readout circuit

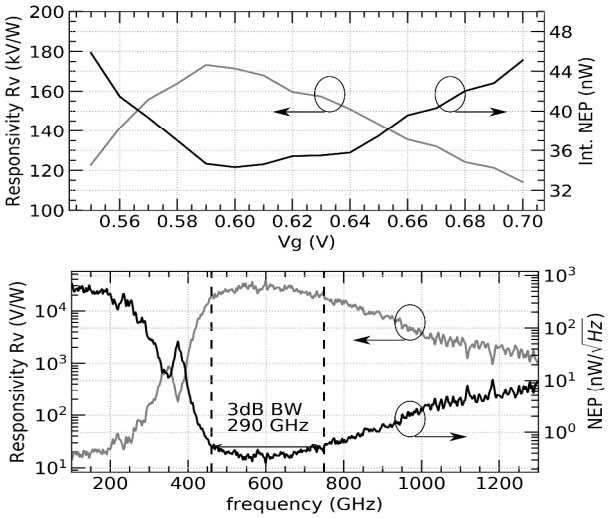

Figure 34.3.4: Measured video-mode performance at 0.653THz [top], and chopped single-pixel performance across the wide RF band [bottom].

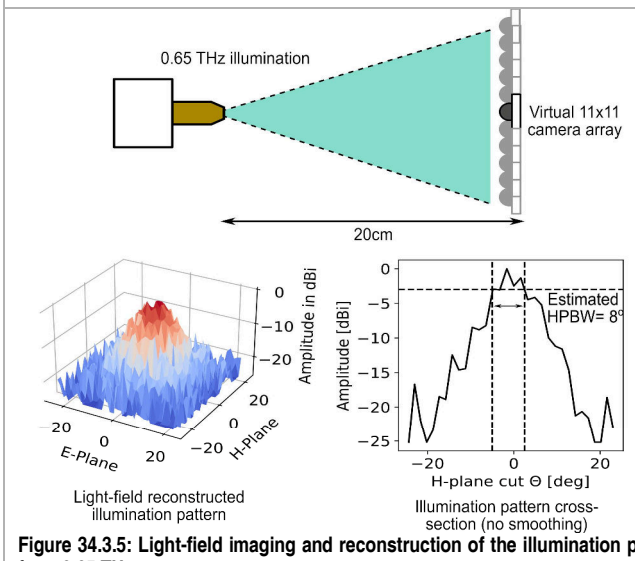

Figure 34.3.5: Light-field imaging and reconstruction of the illumination pattern from 0.65 THz source

	This work	JSSC 2012 [4]	ISSCC 2019 [5]	Sensors 2016 [6]	A-SSCC 2018 [7]
Process	130nm CMOS	65nm CMOS	180nm CMOS	130nm CMOS	180nm CMOS
Array size	32x32	32x32	32x32	31x31	32x24
Pixel pitch	80µm x 80µm	80µm x 80µm	215µm x 215µm	240µm x 240µm	220µm x 200µm
Power consumption	13.3µW/pixel*	2.5µW/pixel	4.5µW/pixel	174µW/pixel	-
Operation frequency	460-750GHz**	790-960GHz**	930GHz	200GHz, 270GHz, 600GHz	860GHz
Antenna	Rectangular wire-loop	Ring	Patch	Bow-tie	Patch
On-chip gain	139dBΩhm + PGA 7-51dB	50dB	45dB	31-71dB	24dB
NEP	36nW (int.) @ 653GHz, 262pW/Hz$^{0.5}$ @ 653GHz, 40kHz chopping	12nW (int.) @ 860GHz, 100pW/Hz$^{0.5}$ @ 860GHz, 5kHz chopping	91pW/Hz$^{0.5}$ @ 930GHz, 31Hz chopping 13.7 pW/Hz$^{0.5}$ @ 930GHz, 100kHz chopping	533pW (int.) @ 270GHz, 156kHz chopping 732pW (int.) @ 600GHz, 156kHz chopping	-
ADC	On-chip, 6b FADC	External	On-chip, 4x12b	External	On-chip, I-ADCs
Data interface	SPI	Analog	4x12b parallel	Analog	32 parallel I-ADCs
Readout chain	On-chip	External	On-Chip	On-chip	On-chip
Operation mode	CW	CW	Modulated	Modulated	CW
Frame rate	25fps	25fps	400fps	25-100fps	25fps
Optics	Si-lens	Si-lens	None	None	None
Light-field mapping	Yes	Yes	None	None	None

* Average including power consumption in complete readout chain and digital logic
** 3-dB NEP bandwidth

Figure 34.3.6: State-of-the-art comparison table for large pixel count silicon integrated THz cameras

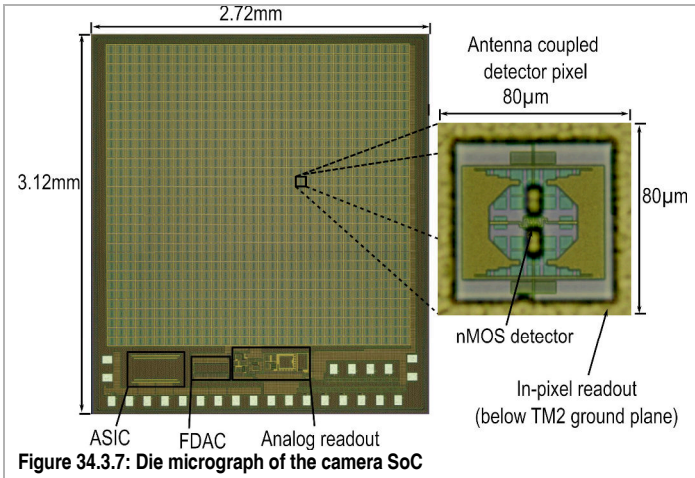

Figure 34.3.7: Die micrograph of the camera SoC