A 64-Pixel 0.42-THz Source SoC With Spatial Modulation Diversity for Computational Imaging

Ritesh Jain, Philipp Hillger, Eamal Ashna, Janusz Grzyb, Ullrich R. Pfeiffer

IEEE Journal of Solid-State Circuits
https://doi.org/10.1109/JSSC.2020.3018819

A 64-Pixel 0.42 THz Source SoC with Spatial Modulation Diversity for Computational Imaging

Ritesh Jain, Philipp Hillger, Eamal Ashna, Janusz Grzyb, and Ullrich R. Pfeiffer, *Fellow, IEEE*

(Invited Paper)

***Abstract*—This paper presents a terahertz source system-on-a-chip (SoC) specifically designed for computational imaging with a single pixel camera (SPC). The SoC consists of an 8×8 array of independent, frequency unlocked THz sources that together radiate maximum 10.3 dBm power at 0.42 THz. Each source pixel is composed of a fundamental Colpitts oscillator, followed by a common-collector doubler, and an on-chip circular slot antenna. The THz power radiated from the array can be modulated in space by turning the pixels on or off individually with 100% modulation depth. The SoC integrates a dedicated memory space where 64 of such spatial patterns can be stored and triggered externally at up to 10 MHz modulation rate. The spatial modulation can be additionally multiplexed with separate programmable chopping rates for individual pixels. The combined modulation diversity provides a highly reconfigurable THz light projection for SPCs. Furthermore, each pixel also incorporates a built-in power-test (BIST) for an in-situ radiation power monitoring and calibration. All of the aforementioned functions are programmable with an integrated ASIC through a standard SPI interface. This integration level readily allows low-cost aperture scaling by combining multiple chips at the board level. The SoC was applied in a compact, 8×8 pixel, silicon-only THz SPC which captures transmission mode images at 25 frames per second with 40 dB voltage dynamic range. With an appropriate receiver and baseband processing, the imaging speed of such SPCs can be extended to thousands of frames per second.**

***Index Terms*—spatial light modulator, SLM, single pixel camera, terahertz source, source-array, system-on-a-chip, SoC, computational terahertz imaging, reciprocal imaging, modulation diversity, reconfigurable, high power, terahertz radiator, incoherent source.**

I. Introduction

TERAHERTZ (THz) radiation is a promising candidate for industrial radiography and many other non-destructive imaging applications due to its several unique and interesting properties [1]–[4]. Silicon integration has always been appealing for THz imaging systems for it offers benefits including the economies of scale, monolithic system integration, portability, and low power consumption for full SoC integration [5]. Detailed reviews of the current state-of-the-art in silicon integrated THz imaging and sensing systems can be found in [6], [7]. In [6] a typical radiation power of 0 dBm (1 mW) has been reported for a SiGe HBT THz illumination source array at around 0.5 THz. Single detector sensitivities have been reported in the range of -150 dBm/Hz and -80 dBm/Hz$^{0.5}$ for Si-integrated heterodyne and direct detectors respectively. Silicon components can therefore now offer a maximum 150 dB of dynamic range (DR) for THz imaging. However, such performance can only be achieved when all the source power is focused at a single point which is mechanically moved across the object cross-section; and a heterodyne detector captures each pixel with one second integration period in succession. The imaging consequently slows down to an impractical rate of minutes per frame. To improve the imaging speed, the detection can be parallelized using multiple sensors, and many THz focal-plane arrays (FPAs) have been reported in the literature [8]–[10]. Such integration however is achieved at the cost of sensitivity. Only direct power detectors can be densely integrated on a chip, as more sensitive heterodyne detectors require complex EM structures, larger footprints, and larger dc power [6]. The FPA integration further includes a signal readout chain which adds more noise. The full aperture illumination also gets diluted over multiple FPA pixels resulting in further DR degradation in these imaging setups. Multiple source elements, both mutually locked [11], [12] and unlocked [13] in phase, have also been implemented in silicon technology to increase the radiated THz power. While the phase-locked or coherent sources can be leveraged to extract 3-D ranging information [14], they also add interference speckles to the images [15], [16]. THz phased arrays such as those presented in [17], [18] can additionally facilitate electronic beam-steering for a faster object scanning. However, the implementation of such sources has remained challenging due to the current silicon technology limitations, and little research has been carried out on their limited scalability and directivity (see Table I). All such imaging systems are therefore constrained to incremental improvements that are bound to the slow technology progress.

A single-pixel camera (SPC) is a non-conventional imaging system that approaches the source and detector relationship in a converse manner. In SPC, the incident incoherent illumination itself is divided into multiple pixels, and the image is acquired with a single detector unit. Several sequential measurements are taken at the receiver by modulating the illumination pixel amplitudes into spatial patterns, and the image is reconstructed computationally from the measured data. This is usually accompanied by a sparse computation technique called compressive sensing (CS) for reducing the number of sequential measurements and thus speeding up the imaging process [19]. SPC is appealing for any frequency range where sensitive detector FPAs are inaccessible, or where a much more sensitive single detector pixel is instead available. THz radiation also falls into this category, as the sensitivity of a single heterodyne THz

This work was funded by the German Research Foundation (Deutsche Forschungsgemeinschaft, DFG) under the individual grant project 'Silicon Integrated Smart Terahertz Source Arrays for Reciprocal Imaging (SI-STAR)'.

The authors are with the Institute for High-Frequency and Communication Technology, University of Wuppertal, Wuppertal 42119, Germany (email:rjain@uni-wuppertal.de, ullrich@ieee.org).

Digital Object Identifier (DOI): 10.1109/JSSC.2020.3018819

receiver is orders of magnitude higher than a direct detector, and a single pixel direct detector is still more sensitive than an FPA [6]. Therefore, a THz SPC can relax the implementation issues associated with the high power sources and the low-noise FPAs. Many THz SPC systems have been reported in the recent years. In [20], PCB masks with 32×32 pixels were used with an external fiber-coupled pulsed THz source. Hundreds of masks were replaced manually to create spatial patterns for a THz SPC demonstration at 100 GHz. A THz spatial light modulator (SLM), constructed as an 8×8 pixel active metamaterial array with n-doped GaAs switches, was used along with a Mercury arc lamp THz source in [21]. Here, with a 12 MHz modulation speed and 10% modulation depth of the SLM, an imaging rate of 1 frame-per-second (fps) was demonstrated. More recently, GaAs pHEMT metamaterial switches with 36% modulation depth and 10 MHz modulation speed [22], and micro-machined metasurfaces for broadband 0.1–1.5 THz power switching with 70% modulation depth and 20 kHz modulation speed [23] have also been demonstrated. In another approach, an optical light pattern is projected onto a semiconductor wafer placed in the THz beam path to create plasmonic spatial switching. A 0.35 THz SPC system consisting of an off-the-shelf waveguide based THz source, halogen visible light source, commercial digital light projector (DLP) with 1024×768 pixels, and a Germanium wafer as plasmonic THz switch was demonstrated in [24]. Here, a modulation depth of 45% and a modulation speed of 333 Hz (3 ms pattern period) were reported. In [25], a more general SPC system, originally called a reciprocal imaging system, was proposed. Here, the authors envisioned encoding the illumination pixels with different chopping frequencies for identification and decoding at a single receiver for a fast image acquisition. To the best of our knowledge, such SPCs have not been demonstrated experimentally in the past. Together these techniques are the types of computational THz imaging (CTI) systems that rely on computation intensive or mathematical techniques to form THz images. All the existing THz SPC systems use a single THz radiation source with external spatial modulators. This is beneficial in terms of the radiation bandwidth as THz generation and modulation are decoupled. However, the limited modulation depth and modulation speed of these external modulators adversely impact the image DR and the frame-rate, respectively. The complex nature of such SPC systems also contributes to their high cost, large power dissipation, and poor scalability towards higher pixel count or larger apertures, thus prohibiting any practical deployments.

This paper presents a novel THz source system-on-a-chip (SoC) for CTI that combines a high power incoherent THz light generation with fast amplitude and frequency encoded spatial modulation, and in-situ power calibration. The SoC consists of 8×8 array of free-running, unlocked oscillator based source pixels with individual on-chip antennas. Together, they radiate a maximum power of 10.8 mW (10.3 dBm) at 0.42 THz. The SoC can project arbitrary spatial illumination patterns with 100% modulation depth and a modulation speed up to 10 MHz. The integrated ASIC allows on-chip caching of 64 illumination patterns for faster pattern reconfiguration. Different source pixels can also be simultaneously encoded with non-identical

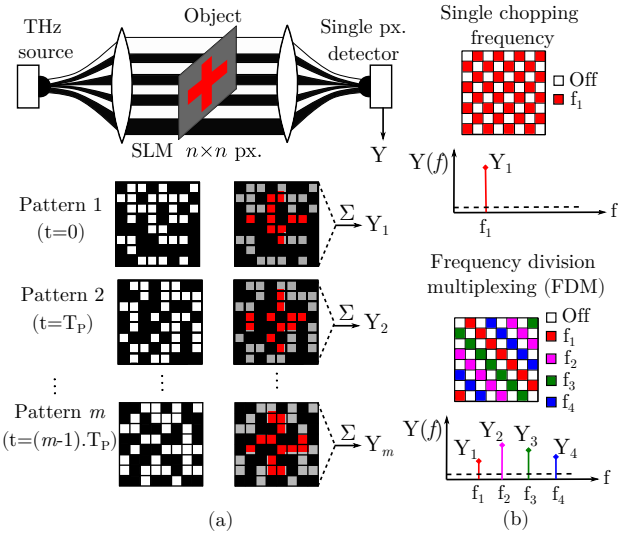

Fig. 1. (a) Conceptual diagram of a transmission mode THz SPC with a binary SLM source and a direct power detector. Here m sequential measurements are done with the switching period T_P between different spatial patterns. (b) FDM concept. Different pixels can be chopped at different frequencies (color-coded) for their simultaneous acquisition in the detected signal spectrum.

chopping frequencies multiplexed over the spatial pattern. Each pixel further incorporates a built-in self-test (BIST) for radiation power monitoring which can be used to calibrate any pixel power non-uniformity or mutual pixel coupling. All of the above mentioned features are programmable through an integrated standard SPI interface, thus allowing a scalable system architecture where multiple SoCs can potentially be assembled on a single board for higher pixel count or to implement larger aperture CTI systems. Note that the SoC was initially introduced in [26]. In this work, the on-chip dc power routing has been further modified for an improved performance. Detailed analysis of the the SoC design aspects and characterization are also presented. Finally, a compact silicon-only 8×8 pixel THz SPC with video-rate imaging at 25 fps (limited by the detector readout) is demonstrated.

The outline of this paper is as follows. Section II reviews the CTI techniques to understand the design requirements for an integrated THz source. The SoC architecture thereafter is detailed in Section III. The circuit design is presented in Section IV, and a brief discussion on the chip packaging is presented in Section V. The experimental results from system characterization and imaging demonstration are presented in Section VI, and the conclusions are derived in Section VII.

II. Computational Terahertz Imaging with Single Pixel Camera

This work proposes to combine the generation and spatial modulation of the THz radiation in a single source module. The conceptual diagram of a THz SPC system incorporating such a source is shown in Fig. 1(a). Here, a transmission mode setup is assumed with a generic $n\times n$ pixel source-array SoC and a single-pixel direct power detector. The radiated output power from each individual pixel of the source SoC can be binary modulated with 100% modulation depth. Any arbitrary

arrangement of pixels switched either on or off individually forms a spatial illumination pattern. This is transmitted through the object, and integrated over the angular aperture of the detector. Assuming incoherent integration of pattern power within the linear operation region of the detector, its output voltage Y can be expressed as

$$Y = R_v P_o \cdot \sum_{k=1}^{n^2} \phi_k \alpha_k \tag{1}$$

where k is the linear equivalent vector index for the 2D pixel matrix of size n×n. It is assumed that all pixels radiate the same power P_o and the switching status of k^{th} pixel is denoted by $\phi_k \in \{0, 1\}$. The fraction of radiation power transmitted through an object cross-section in path of the k^{th} pixel is denoted by α_k. Therefore, the detector receives a THz radiation power $P_o\phi_k\alpha_k$ from the pixel which is converted into a signal proportional to the detector responsivity R_v. The net output signal Y is the superposition of signals detected from all pixels. However, a single measurement as denoted in Eq. 1 cannot distinguish between the individual pixels. The SPC applies illumination restructuring for image formation. In particular, different spatial patterns are projected in succession (e.g. with a pattern switching period T_P) and a measurement vector is gathered. For m number of projected patterns in a total time $(m-1)T_P$, the process can be denoted as,

$$\begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_m \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} & \cdots & \phi_{1n^2} \\ \phi_{12} & \phi_{22} & \cdots & \phi_{2n^2} \\ \vdots & \vdots & & \vdots \\ \phi_{m1} & \phi_{m2} & \cdots & \phi_{mn^2} \end{bmatrix} \cdot \begin{bmatrix} X_1 \\ X_2 \\ \vdots \\ X_{n^2} \end{bmatrix} \tag{2}$$

or,

$$\boldsymbol{Y}_{m\times 1} = \boldsymbol{\Phi}_{m\times n^2} \cdot \boldsymbol{X}_{n^2\times 1} \tag{3}$$

where each row vector in the pattern matrix $\boldsymbol{\Phi}$ indicates a spatial pattern. The vector $\boldsymbol{X}$ is the required image signal indicating the fraction of power transmitted by the object cross-section. Compared to Eq. 1, the signal notation is simplified as $X_k = P_o R_v \alpha_k$. As the pattern matrix $\boldsymbol{\Phi}$ and the measurement vector $\boldsymbol{Y}$ are known, the image vector $\boldsymbol{X}$ can be calculated after the measurement as

$$\boldsymbol{Y}_{m\times 1} \cdot \boldsymbol{\Phi}^{-1}_{m\times n^2} = \boldsymbol{X}_{n^2\times 1} \tag{4}$$

which can be rearranged into an n×n matrix to render a 2D image.

For a deterministic image, $\boldsymbol{X}$ must be a unique solution. This requires a square pattern matrix $\boldsymbol{\Phi}$ with a full rank and non-zero determinant. Therefore, for a minimum deterministic pattern sequence, the number of patterns m should be equal to the total number of pixels n×n. For example, $\boldsymbol{\Phi}$ can be an identity matrix denoting a time division approach where the object is pixel-wise scanned. Some other matrices also exist where more than one pixel can be switched on in each pattern. Note that signal Y is proportional to the number of pixels switched on in a pattern. Therefore, the SNR at the detector increases with increasing number of 1's in $\boldsymbol{\Phi}$. The required measurement time is proportional to the number of pixels and the pattern switching period. Furthermore, most SLMs, including ours, provide a binary modulation. Many computation techniques show higher sensitivity for the phase-intensity modulation i.e. $\phi \in \{-1, 0, 1\}$, which can be approximated by subtracting two binary spatial patterns [21]. CS techniques are further used to approximate the solution to Eq. 4 for a non-square $\boldsymbol{\Phi}$, i.e. for fewer patterns as compared to the number of pixels, thus increasing the frame-rates [19]. Ideally, a single pattern can also yield a binary decision for object identification, essentially acting as an optical neural network [27]. In all these case, the fast pattern switching is crucial for high-speed imaging. A higher radiation power from each source pixel still benefits the image DR. In practice, each of the pixels produces a slightly different power level which is further deteriorated by the aberrations of the optical system. A calibration image is therefore required to correct for such non-uniformity [24]. However, this does not differentiate between the source pixel non-uniformity and optical aberrations. The pixels can further show some level of undesired mutual power coupling. Therefore, BIST for each individual pixel power therefore becomes crucial to calibrate the resulting artifacts.

For continuous-wave (CW) radiation, the signal power is integrated over time at the detector. A longer integration period reduces the readout noise bandwidth and thus improves the detector sensitivity, which is contradictory to a shorter pattern switching period required for faster imaging. Such trade-off can be mitigated with a chopped readout. Here, radiation from the source pixels is chopped at frequencies above the flicker noise corner of the detector, and a digital signal processor (DSP) samples the image signal to extract its spectrum and filter out the noise. The chopping frequency-division multiplexing (FDM) scheme is hereby proposed which can improve the imaging speed further. This is shown in Fig. 1(b). If different pixels can be chopped simultaneously at different rates, their image response can be acquired from the readout spectrum at the same time. In Fig. 1(b), four mutually exclusive patterns are multiplexed over four non-overlapping chopping frequencies which are sampled in the same spectrum. In the case of square-wave chopping, such non-overlapping frequencies can be, for example, placed between the first and the third harmonics of the lowest chopping frequency. This is specially useful large pixel count SPCs, as the number of measurements can be directly reduced in proportion to the number of frequency tones applied for the chopping FDM. However, if a large number of tones are employed simultaneously, a fine frequency resolution is required. This, in turn, necessitates a large number of samples, thus degrading the temporal resolution. Next, fewer 'on' pixels in a chopping tone encoded spatial pattern translates to a lower integrated signal power at the detector with inferior SNR. The FDM planning ultimately depends on the noise level and bandwidth of the detector, as well as the sampling and readout rates of the DSP. Depending on the available components, FDM can be adapted to optimize the SNR and frame-rates in the SPC.

The proposed SPC approach has an inherent advantage as compared to the traditional imaging approach (i.e. single source element combined with a detector FPA such as [8]). A source array which combines spatial modulation permits increasing

the number of pixels for the SPC imaging aperture without degrading the SNR. In the traditional approach, the power incident on the FPA is fixed and thus divided evenly among the FPA pixels. Therefore, if the FPA pixel count is increased by a factor of 10, the imaging SNR drops by a factor of 10 dB. This is not the case for the SPC approach as the power per pixel ideally remains constant when the number of pixels is increased at the source array.

All the techniques from above work equally well with a heterodyne receiver. Since the source pixels are frequency unlocked, their radiation frequencies are at mutual offsets with incoherent phases. A heterodyne detector recognizes the net impinging power as an frequency envelope with an IF bandwidth centered around the mean source frequency. Integration over a sufficient IF bandwidth accommodating the complete envelope baseband-equivalent spectrum results in an output signal Y as given by Eq. 1. With FDM, the LO frequency at the detector can be modulated at different rates for the lock-in acquisition of different chopping components. Since a single heterodyne receiver pixel is sufficient, a III-V technology integrated receiver can be preferred over silicon-integrated receiver for even better sensitivity [28]. Detailed investigation into these different CTI modalities is however beyond the scope of this manuscript. This paper focuses on the design of a THz source SoC enabling all such diverse imaging techniques in a silicon integrated circuit for the first time.

III. SoC Architecture

The primary considerations influencing the source SoC design are already outlined in the previous section. Such source should provide a high radiation power with fast pattern reconfiguration rate, pixel-wise BIST power monitoring, and chopping FDM functionality. Additionally, a 2D imaging system benefits from a large number of pixels for dense spatial sampling. Integrating hundreds of source pixels in a large SoC quickly becomes prohibitive due to the cost, variability, and thermal bottlenecks. The dc power consumed by multiple source pixels quickly leads to a thermal throttling of the RF power. Due to a larger bias current, the IR voltage drop along the shared bias lines also becomes prohibitive to a uniform biasing along the array. Additionally, the chip fabrication cost increases rapidly due to an increase in the chip area. A larger chip also requires a larger silicon lens which further adds to the cost. Therefore, integrating large number of source pixels on a single chip follows the law of diminishing returns in terms of the cost economics and the net radiated THz power output. Considering these limitations, we have restricted our source array integration to 8×8 pixels. For scaling the source further towards large aperture, high pixel count systems, we expect that assembling multiple SoCs on a single printed circuit board would be a more feasible approach. In this anticipation, the SoC is also equipped with a standard, sharable programming interface and common dc bias lines.

The SoC block diagram is shown in Fig. 2. The RF front-end of each individual source pixel is composed of a free-running fundamental oscillator followed by a frequency doubler, feeding an on-chip antenna. This RF architecture

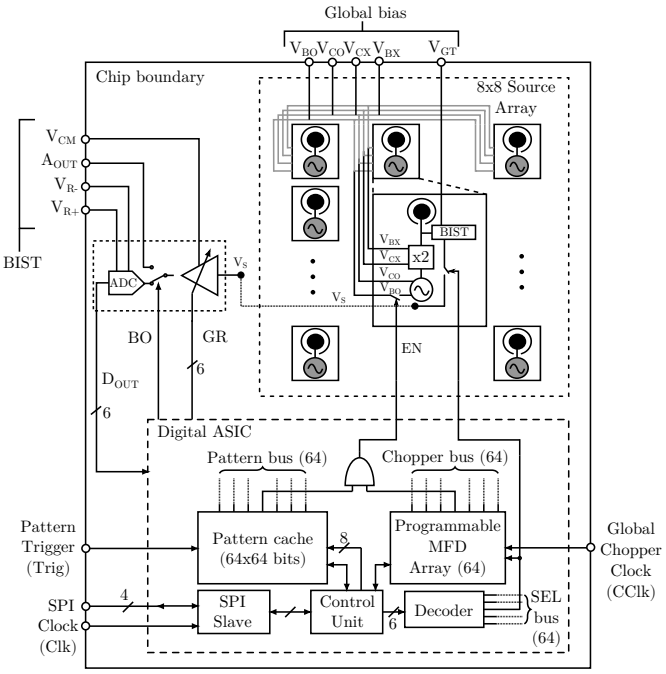

Fig. 2. Block diagram of the 8×8 pixel THz source SoC with global biasing, BIST monitoring, and an SPI interface. External trigger (Trig) is used for projecting the next cached pattern from the memory, and global clock (CClk) with 64 element MFD array performs the FDM.

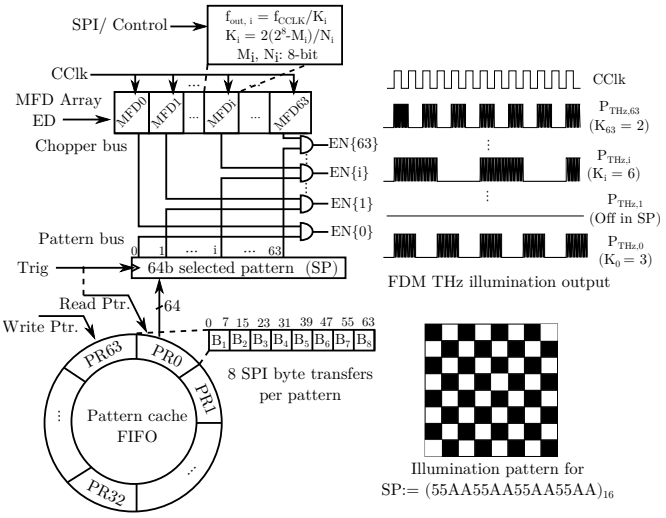

Fig. 3. Digital programming model for the SoC. The 64-pattern cache memory is configured as a circular FIFO. Working pattern is triggered into 64-bit SP register, which is bitwise-ANDed to a reconfigurable 64-element MFD array, thus providing different chopping frequencies for each pixel.

allows a robust and high power THz signal generation [29]. The antennas are designed to radiate from the chip backside into a hyper-hemispherical silicon lens, which serves many purposes. First, it allows high directivity, non-overlapping source beams, and second, it suppresses the propagation of RF substrate modes to minimize the RF cross-coupling and frequency pulling between different pixels [30]. Also, the antenna area is reduced by about an order of magnitude, since the lens allows backside radiation through a higher permittivity medium (silicon, $\epsilon_{Si} = 11.7$) instead of air. The mitigation of

substrate modes allows a high efficiency, well-defined, and non-overlapping Gaussian radiation pattern for each pixel. Therefore, the lens permits a dense integration of the 64 source pixels [31]. Note that the saving in chip area more than compensates for any additional cost of the lens. For example, a CMOS integrated 32×32 0.9 THz FPA with front-side radiating patch antennas in [9] consumes 100 mm^2 chip area, while a similar pixel count FPA with ring antennas radiating from the backside into the silicon lens in [8] consumes 10 mm^2 of chip area.

Four dc biases, two for the oscillator (V_{BO}, V_{CO}) and two for the doubler (V_{BX}, V_{CX}) are required for each pixel. These biases, supplied globally, are shared among the pixels with low resistance (0.3Ω/mm) dc lines. Note that the chip sinks up to 1.6 A current from V_{CO}. In the absence of a low resistance routing, different spatial patterns may sink different currents, resulting into different IR drops which may generate a large mutual dc coupling between the pixels. This was also the case with the chip presented in [26] where a bus routing scheme was used for the supply lines. In this paper, a modified chip is presented with an improved mesh type dc routing which distributes the current more evenly for a minimal voltage drop. Each pixel also integrates an NMOS square-law detector near the antenna feed for an in-situ BIST monitoring of the radiated power. The detector bias for all pixels is shared with a global pin V_{GT}. All BIST outputs are multiplexed to a common readout composed of a programmable gain amplifier (PGA), with an output switchable to either an external monitor signal A_{OUT}, or an integrated 6-bit flash ADC readout. The decoder logic is used to select the pixel for BIST monitoring. The common mode bias for the PGA (V_{CM}) as well as the ADC range voltages (V_{R+}, V_{R-}) are supplied externally.

A separate 'enable' flag (EN) available at each pixel is used for power switching. This flag, as well as the the PGA, and the BIST output selection, are all controlled by an integrated digital ASIC backend. The programming model for this ASIC is further elaborated in Fig. 3. Note that sending the 64-bit EN flag data from an external computer to the SoC can suffer from a large programming latency. To facilitate a faster pattern switching, the ASIC comprises a pattern cache memory with 64 different 64-bit pattern registers (PR0–PR63) that can be pre-loaded and projected sequentially. This size of pattern cache is selected to allow a minimum deterministic pattern sequence as discussed in Section II. Also, the pattern registers are arranged in a circular FIFO so that they can be iterated over cyclically once a pattern sequence is pre-loaded. An external trigger signal (Trig) is used to load a pattern from the cache to the selected pattern (SP) register. External triggering is useful for synchronization between the detector signal measurement and the source pattern reconfiguration for systems that may need this functionality.

For chopping FDM, the SP register output is bitwise-ANDed to the outputs of a 64-element modulo frequency-divider (MFD) array to produce 64 EN flags for all the pixels. The MFD is a digital fractional frequency-divider which works on modulo arithmetic. Its frequency-division ratio K is controlled by two 8-bit programmable registers M and N as $K = 2(2^8 - M)/N$ with $2 \leq K \leq 512$. For an even division ratio, the MFD output has 50% duty cycle, while for an odd division ratio the duty cycle is close to 50%. All MFDs share a common global chopper clock (CClk) at their inputs, and based on their individually programmed division ratios, they can produce different chopping frequencies for individual pixels. The MFD array can also be globally disabled via a flag ED.

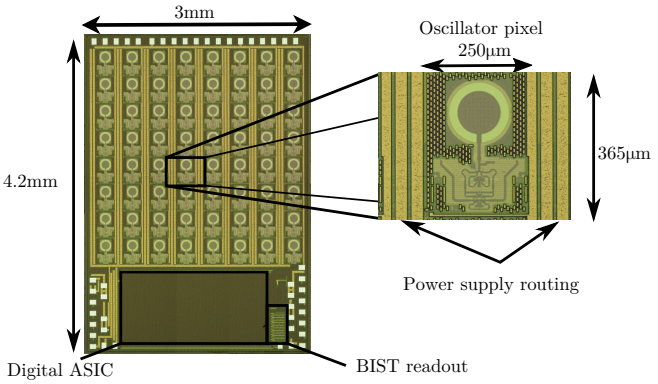

Fig. 4. Die micrograph for the source SoC with a zoom-in view of the oscillator pixel. The chip was implemented in the commercial SG13G2 BiCMOS process available from IHP microelectronics.

The chip micrograph is shown in Fig. 4. It was implemented in a commercial SG13G2 SiGe BiCMOS process available from IHP microelectronics with 350GHz/450GHz f_T/f_{Max} SiGe HBT transistors, 130nm CMOS backend with 1.2 V logic, and 7-layer BEOL stack including five thin (M1–M5), two thick (TM1–TM2) metal layers, and MIM capacitors. The chip area is 12.6mm^2 out of which 9mm^2 and 2.1mm^2 are occupied by the pixel array and ASIC, respectively. The chip thickness is 150 μm. The circuit designs of the source pixel and the BIST are discussed further in the next section.

IV. Circuit Design

The circuit schematic of the source pixel is shown in Fig. 5(a). It is similar to the THz source presented in [29] with a modified layout to fit a compact, square pixel area. The pixel consists of a fundamental differential Colpitts oscillator with an output isolating cascode stage feeding a balanced common-collector doubler. The differential design ensures a minimal fundamental leakage at the doubler output. Also, the doubler is designed to provide a reactive feedback of the second harmonic generated at the transistor's emitter to its base-emitter junction, which allows to boost the second harmonic current. In addition, the doubler provides a high isolation between the antenna and the oscillator core preventing any mutual RF coupling between the pixels. The optimum impedances for the doubler devices were determined from load- and source-pull simulations. Based on this, an interstage matching network comprising TL_S, TL_C, $TL_{1,2}$, C_C, and TL_3 was designed. An output matching network comprises a circular slot antenna whose capacitive input impedance is transformed through TL_4, TL_6 to present the optimum 2nd harmonic termination to the doubler emitter port. The radiating slot aperture of the antenna with 152 μm diameter is created in the common ground plane, with a TM1 circular center patch of 106 μm diameter supporting a linear polarization [29]. To increase the angular coverage of

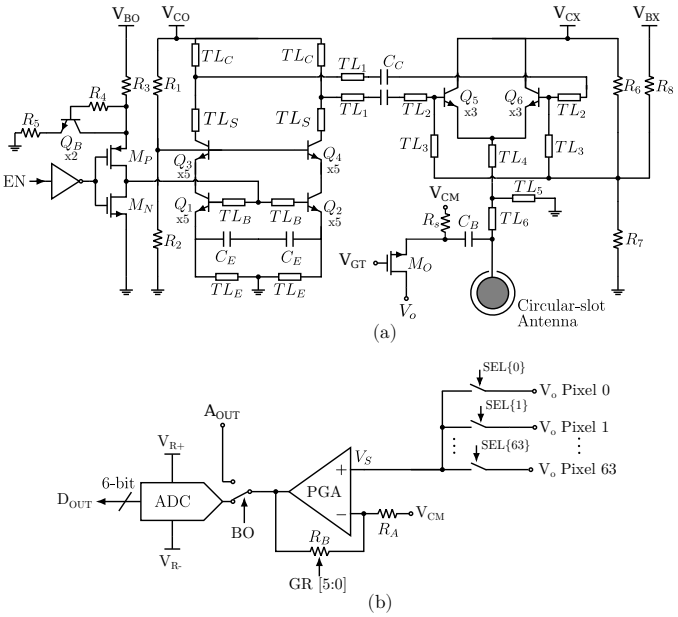

Fig. 5. (a) Source pixel schematic with a differential Colpitts oscillator, CC doubler, switching circuitry, on-chip circular slot antenna, and integrated power detector M_O; (b) shared BIST readout with the PGA and the ADC.

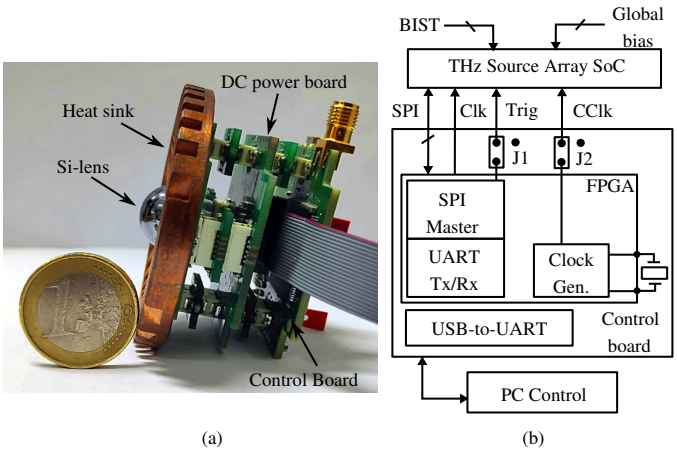

Fig. 6. (a) Packaged source module with a 15-mm Si-lens of elliptic extension and a passive Cu heat sink. A 1-euro coin is shown for scale. (b) Block diagram for the control scheme used to operate the module from a PC.

the source module, the physical design of the source pixels is aimed at minimizing the area consumption of the source elements. All inductors and RF chokes are implemented using microstrip transmission lines. The capacitors are designed in the MIM stack, and a resistive biasing scheme is used throughout. The total area of a single source element is 365×250 μm^2 where 60% of this area is occupied by the antenna. Simulated maximum generated signal power of -1.66 dBm at 439 GHz are observed for V_{BO} of 1 V and V_{CO} of 4.4 V at 27°C ambient temperature. The power and frequency drops to -7.5 dBm and 432 GHz respectively when the ambient temperature is increased to 70°C in simulations. This thermal throttling of radiation power becomes significant when multiple pixels are turned on simultaneously in the array as explained later.

For the pixel switching, the base bias of the oscillator is controlled by an analog switch composed of transistors M_P and M_N. Here, the diode-connected transistor Q_B helps in absorbing any instantaneous switching current at the base to maintain a low ripple V_{BO} bias shared across the array. This minimizes the ac switching related cross-talk between the pixels. The logic level applied at the 'EN' flag pulls the base voltages of Q_1, Q_2 to either Q_B or ground to turn on or turn off the oscillator respectively. The chopping frequency is limited by the time constant of the bias network. In simulations, the oscillation voltage signal at the base reaches 99% of its final amplitude in 6 ns after setting the 'EN' flag.

The 1μm /0.13μm NMOS transistor M_O in a common-gate configuration [8] is used as a power detector for BIST. The detector requires a gate-source bias in the range of 0.25–0.3 V for the optimum responsivity. Here, the 1.3 fF coupling capacitor C_B is composed of a 32 μm^2 MOM stack formed between the antenna feed line on TM1 and M5. A -15.1 dB power coupling is simulated between the antenna and the power detector at around 400 GHz. The source terminal of M_O is biased with voltage V_{CM} in the common-mode range of the readout PGA. The shared readout scheme is shown in Fig. 5(b). The PGA features a common-mode voltage range of 0.3–0.9 V with a simulated voltage gain of 3–29 dB (GBW $\approx$ 1.25 MHz), that is programmable via the resistor bank R_B controlled from a 6-bit gain register GR. Different BIST pixels can be selected with the transmission gate switches SEL for input to the PGA. The output of the PGA can be switched either to the pin A_{OUT} which can be monitored externally, or it can be sampled with an integrated 6-bit flash ADC (measured ENOB $\sim$ 5.85, maximum sampling rate $\sim$ 7.3 MHz) with an externally adjustable voltage range (300 mV–1.2 V). The ADC output is read out with the SPI. The entire digital logic was synthesized using a standard digital design flow.

V. Chip Packaging and Module Integration

The packaged source module is shown in Fig. 6. The SoC is centered at the pixel array and assembled to the backside of a 15-mm diameter hyper-hemispherical Si-lens with a thermal epoxy. The Si-lens has an elliptic extension which results in the calculated field-of-view (FoV) of 68° for the 64 source beams, with a central beam directivity of 36.4 dBi (half power beamwidth, HPBW $\sim$ 2.72°), and a mutual beam separation angle of 7.5°. These calculations follow a similar geometrical model as suggested in [32]. Since the pixels can generate large amount of heat when they are turned on simultaneously, a passive circular copper heatsink of 27 cm^2 area is also attached to help with the heat dissipation. The block diagram for control board is shown in Fig. 6(b). It consists of an FTDI FT232R based USB-to-serial UART interface to control the SoC from an external PC. The UART transmitter and receiver blocks, as well as the SPI master controller are implemented on a Xilinx spartan-6 FPGA. A clock divider block is also provided at the FPGA for generating the 'CClk' signal from the 100 MHz XTAL FPGA clock. The control board is also equipped with the solder jumpers J1 and J2 which can be configured to supply the 'Trig' and 'CClk' signals, respectively, from either the FPGA or an external generator. The PCB boards are attached together with board-to-board connectors. Note that the SoC

doesn't require any external RF component, and a low cost FR-4 board is used for the packaging. The overall dimensions of the packaged module are 5.8×5.8×5 cm^3.

VI. Experimental Results

Different measurement setups were employed for comprehensive characterization of both the individual source pixel and the array. The measurements setups are shown in Fig. 7. The radiation power was characterized with a waveguide horn antenna coupled PM4 Erikson calorimeter available from Virgina Diodes (Fig. 7(a)) as well as a photo-acoustic absolute THz power meter available from TK instruments (Fig. 7(b)). The former shows a sensitivity of -30 dBm. Here the waveguide horn antenna is also capable of rejecting any fundamental harmonic leakage from the source pixels due to the waveguide cut-off frequency. However, the PM4 power meter is also prone to the background infrared radiation and must be calibrated periodically. The TK power meter has a slightly worse sensitivity of -23 dBm for all RF frequencies up to 3 THz, but it provides a superior power collection aperture with 3×5 cm^2 area. Here, the impact of any background infrared radiation is also removed by chopping the source power at 35 Hz and reading it with a lock-in method. The power measurements were performed in the near-field with approx. 1 cm distance between the source and the meter heads. This was done to avoid the dynamic range degradation of the source power associated with the free-space path loss in the far-field (Fraunhofer distance for 1.5 cm Si-lens aperture at 0.42 THz is 63 cm). Radiation frequency was characterized using a ×18 harmonic mixer available from Radiometer Physics as shown in Fig. 7(c). For far-field measurements, the setup shown in Fig. 7(d) was used. Here, a SiGe HBT direct power detector with 700 V/W responsivity and 8pW/Hz^2 noise-equivalent power (NEP) at around 0.43 THz was used for relative power measurements [33].

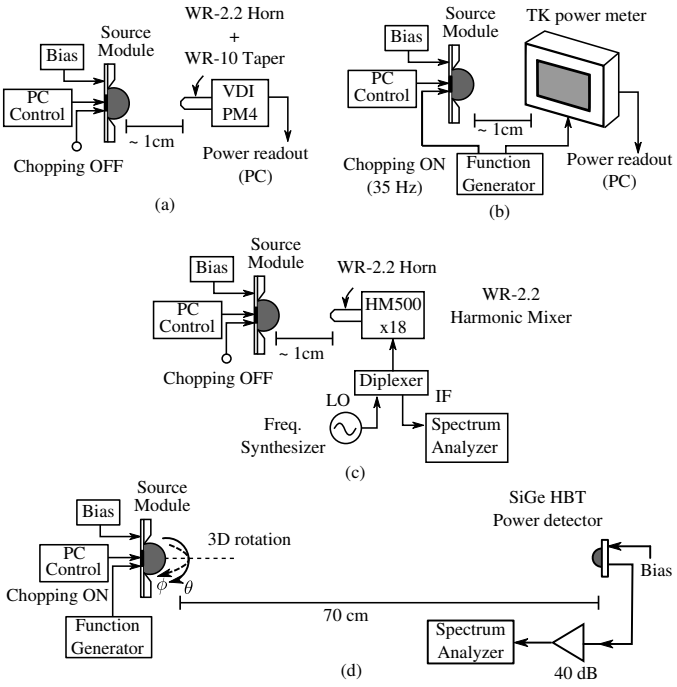

Fig. 7. Different free-space characterization setups used in this work. (a) Power measurements in the near-field with an Erickson calorimeter (PM4); (b) Power measurements in the near-field with a photo-acoustic absolute THz power meter (TK); (c) Frequency measurements with a ×18 harmonic mixer (HM500); (d) Antenna pattern characterization in far-field with a SiGe power detector.

A. Single pixel characterization

For single pixel characterization, only one of the center pixels from the array was turned on and measured. The radiation power and frequency characterization results are presented in Fig. 8. For some bias points, the PM4 and TK measurements do not coincide. At V_{CO} of 4.2 V, the PM4 shows about 38% larger power than TK. The reason for such deviations is suspected to be some standing waves or reflections that might form in the near-field between the metallic horn antenna at PM4 and the Si-lens at the source, despite using THz wave absorbers. Nevertheless, the peak powers observed from both the measurement setups are identical. At V_{CO} of 4.4 V, the peak power is measured as 476.2 μW for the PM4 and 472μW for the TK. This also indicates that there is negligible fundamental leakage from the source pixel, which is expected from the balanced doubler circuit. The peak DC-to-RF efficiency for a single pixel was measured as 0.05% for a 0.9 W power consumption at the source. This includes a 0.8 W static power consumption at the biasing resistors. In the RF frequency characterization, peak radiation frequency of 418–421 GHz was observed for the pixel. The BIST power detector responsivity was also characterized at the measured peak power. The results are shown in Fig. 9. A peak BIST responsivity of 115 V/W relative to the radiated power was observed for gate-source bias of 0.25 V at the power detector.

The radiation pattern of the pixel was characterized with the far-field setup shown in Fig. 7(d). Here the source pixel was chopped at 1 MHz and the detector response signal was readout from a spectrum analyzer. As shown in Fig. 10, the radiation pattern forms a Gaussian radiation beam with a measured directivity of 34.75 dBi and -14 dB sidelobes. Same setup was used to characterize the maximum chopping frequency of the pixel. A high bandwidth transimpedance amplifier was used at the detector readout, and the pixel was chopped using a function generator. The characterization was limited by the 30 MHz bandwidth of the function generator, which translates into a maximum pixel chopping rate of 15 MHz for a minimum frequency division ratio of 2. The relative power levels for different chopping frequencies thus measured are presented in Fig. 11. The source power shows a 3 dB relative roll-off at a chopping frequency of 10 MHz. The gradual roll-off however is also impacted by the function generator bandwidth limits at higher frequencies. Since larger chopping frequencies could not be verified, a 10 MHz chopping related to the 3 dB power roll-off is considered as the conservative maximum limit for the source SoC.

B. Pixel array characterization

For pixel array characterization, first the PVT related output power variation from different source pixels was measured.

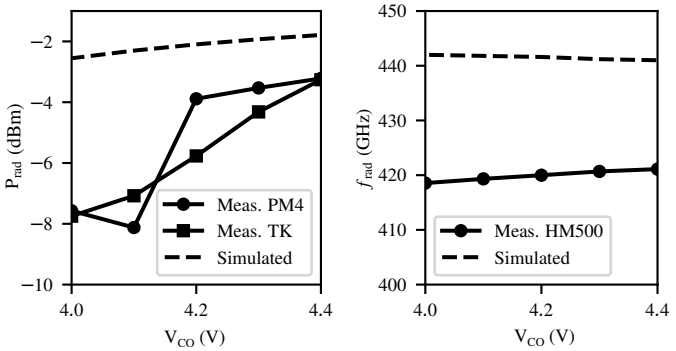

Fig. 8. Measured radiation power and frequency for a single source pixel. The corresponding measurement setups are shown in Fig. 7.

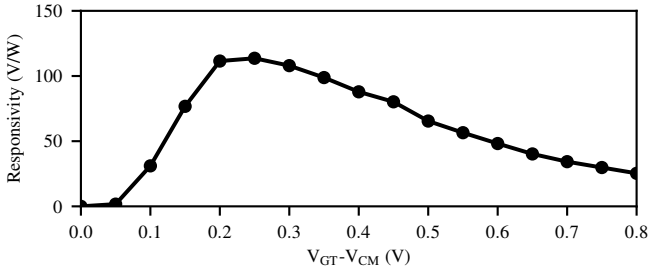

Fig. 9. Responsivity versus bias for the BIST power detector measured with a PGA voltage gain of 3 dB (GR = 1).

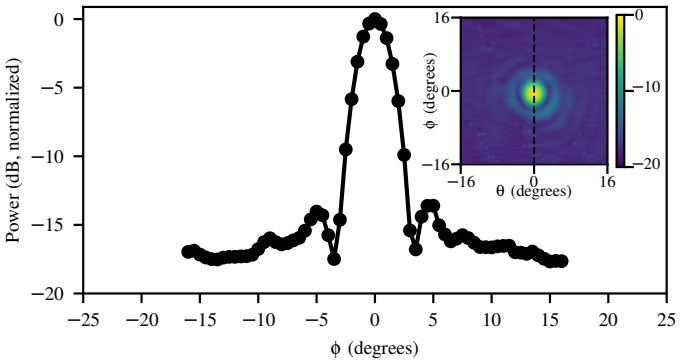

Fig. 10. Measured radiation pattern for a single pixel along the E-plane. Inset shows the azimuth-view of the radiation pattern measured for a 32°×32° angular range.

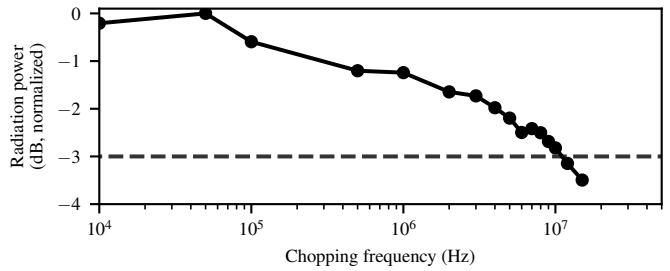

Fig. 11. Relative radiation power vs. chopping frequency for a single pixel, measured with the setup shown in Fig. 7(d). Dashed line marks the -3dB level.

The BIST power monitoring functionality was used for this purpose. Fig. 12 shows the BIST signal detected from each of the 64 pixels turned on separately. This indicates that the

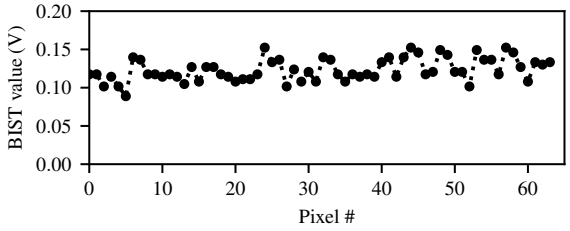

Fig. 12. BIST response measured individually for each of the 64 pixels with PGA voltage gain of 7.2 dB (GR = 2).

pixel power variation is within 3 dB across the array. Note that this also includes the PVT variations that may arise among different detectors. However, the detector responsivity variation, even in large pixel count CMOS integrated FPAs, has been found to be much smaller (e.g. within 1 dB in [34] for 1k-pixel 65nm CMOS detector array when the lens off-axis related roll-off is disregarded. A 3 dB power variation is also within the empirically expected range for such on-chip THz oscillators. More importantly, this result suggests that the shared dc bias is distributed evenly across all the pixels since the power variation is uncorrelated with the pixel position.

Fig. 13 shows the power measured from the array when the pixels are turned on cumulatively. Due to a large FoV of the source, such measurement can only be performed with the TK power meter in Fig. 7(b) as it provides a large power collection aperture. The trend shown in Fig. 13 indicates that radiation power initially scales linearly with the number of 'on' pixels. A linear fit over initial ten pixels yields an average power of 472μW (-3.54 dBm) per pixel which matches to the single pixel power measurements in Fig. 8. However, the measured power drops by 1 dB as compared to the expected linear behavior after 24 pixels are turned on, and a saturation trend is observed thereafter. Identical saturation is also observed in a proxy power indicator composed of the BIST response signal sum over the whole array. This ensures that the saturation is not an artifact from the power meter itself. The saturation arises due to the thermal throttling of radiation power, which can be verified with the thermal imaging of the source module as shown in Fig. 14. Even when 32 pixels are turned on, and the source module is chopped globally at 1 MHz with 50% duty cycle, consuming 2.8 W of average dc power, the lens temperature reaches 55°C. When all the pixels are turned on with 1 MHz global chopping and 4.5 W average dc power, the lens temperature exceeds 67°C. As explained in Section IV, the circuit simulations predict that the peak power from a pixel drops by more than 8 dB at such ambient temperatures. The actual un-chopped dc power and DC-to-RF conversion efficiency for cumulative pixel switching is shown in Fig. 15. The SoC consumes a maximum 6.85 W of dc power when all the pixels are turned on. Here, a peak radiation power of 10.8 mW (10.3 dBm) and the corresponding efficiency of 0.17% are observed. The peak efficiency of 0.24% is reached near the 1 dB compression point (24 pixels), with corresponding dc and RF power of 3.4 W and 8 mW respectively.

Please note that the power saturation should not be considered as an argument against the pixel integration. The

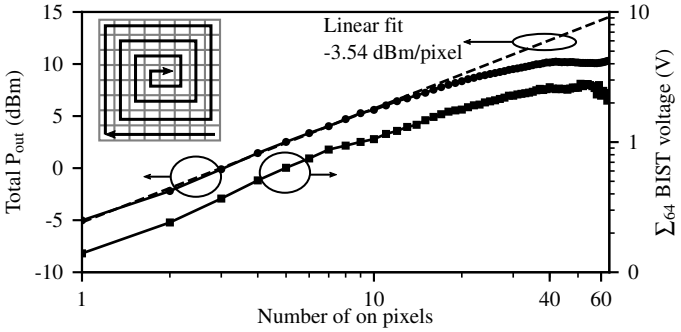

Fig. 13. Net radiation power for cumulative pixel switching, measured with the setup shown in Fig. 7(b). Inset shows the pixel switching sequence. A 30 seconds cool down period was maintained between two subsequent patterns. Dashed line shows a linear fit over ten initial pixels. Right Y-axis shows the corresponding BIST response signal sum over the whole array measured with PGA voltage gain of 7.2 dB (GR = 2).

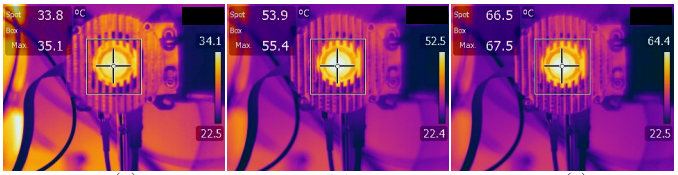

Fig. 14. Thermal images of the source module with 1 MHz global chopping for three different operation states: (a) no pixel turned on (P_{DC}=0.8 W); (b) 32 alternate pixels turned on (P_{DC}=2.8 W); (c) all pixels turned on (P_{DC}=4.5 W).

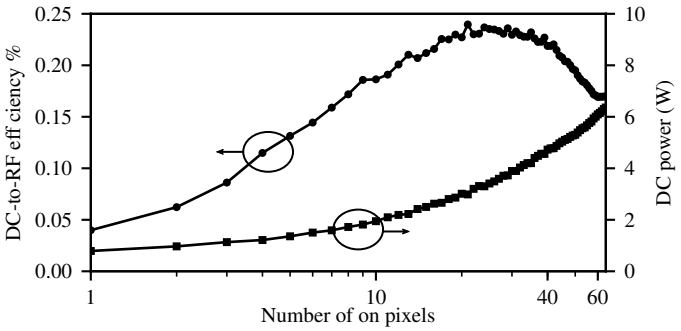

Fig. 15. Overall dc power consumption and DC-to-RF conversion efficiency for the cumulative power measurement shown in Fig. 13.

primary goal of integrating more source pixels on a chip is to increase the spatial extents and resolution of the imaging aperture. The linear power region can still be maintained when the array is operated at less than 50% pixel sparsity with global chopping. However, if more pixels are integrated in the SoC, even fewer fraction of pixels can be turned on simultaneously before running into thermal saturation. Multi-chip scaling can be beneficial here, as the heat can be dissipated from each chip separately. Active cooling solutions can also be used to further maintain the chip temperature.

The measured far-field antenna pattern for the full SoC when all 64 pixels are turned on simultaneously is shown in Fig. 16. It was also measured with the setup shown in Fig. 7(d). All the pixels were chopped globally at 1 MHz. To avoid any thermal issues, the chip was allowed to cool down for 20s before taking a measurement at each point. The antenna pattern shows

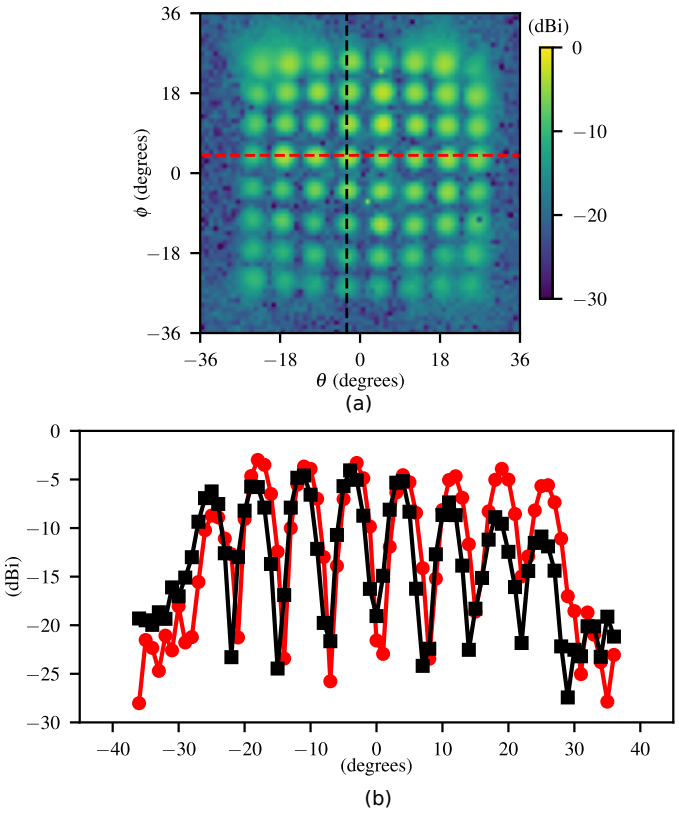

Fig. 16. (a) Measured far-field antenna pattern for the whole array, and (b) Normalized radiation power along the cuts marked in (a).

all 64 source pixels with non-overlapping gaussian profiles and uniform angular spacing. The isolation between individual far-field beams is more than 20 dB. The pixels away from the center also show a lower directivity due to the off-axis behavior of the silicon lens [35]. As shown in Fig. 16(b), the pattern shows an FoV of around 50° from the first pixel peak to the last pixel peak along the orthogonal axes, which translates into an FoV of $\sqrt{2} \cdot 50° = 70.7°$ along the array diagonal. This matches closely to our theoretically calculated FoV of 68°. The central mutual beam separation angle is also close to the theoretical beam separation of around 7.5° [32].

C. SPC imaging

The source SoC was applied for a transmission mode SPC system to demonstrate its imaging capabilities. The optical setup diagram is shown in Fig. 17(a). A SiGe HBT based broadband THz power detector operating in the saturation region with a responsivity of 700 V/W and the noise-equivalent power (NEP) of 8 pW/Hz$^{0.5}$ at around 0.43 THz was used as the single pixel receiver [33]. Note that the detector was empirically observed to be linear for the methods presented here, and is therefore assumed as such. Discussions on any computational complexity associated with the detector response saturation that may arise for different spatial patterns are beyond the scope of the current work. The detector response was read out with a 40 dB voltage amplifier followed by a spectrum analyzer to capture the baseband spectrum $Y(f)$. F-number matched PTFE lenses with 5 cm aperture were used in a collimated beam

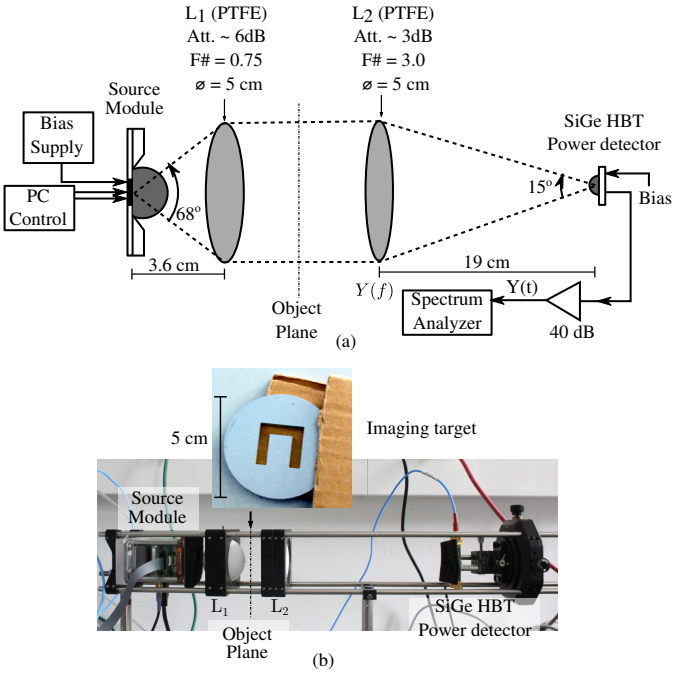

Fig. 17. (a) Optical setup diagram for the SPC. (b) Actual picture of the SPC including the source module, single pixel detector, and PTFE lenses. Inset shows the imaging target which was an aluminum stencil concealed between two cardboard sheets.

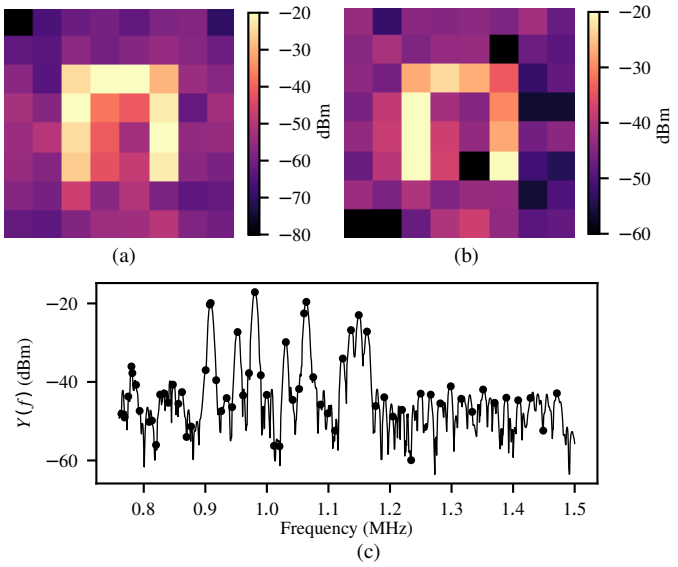

Fig. 18. (a) Image created with single pixel switching (acq. time $\sim$ 100ms); (b) Image created with full FDM modulation (acq. time $\sim$ 40ms); (c) Baseband spectrum for full FDM modulation used to create the image in (b). Dots indicate the received power from different pixels at different chopping frequencies. The signal levels in dBm are the real values observed at the spectrum analyzer.

setup to cover 68° FoV at the source and 22.2 dBi directivity associated 15° FoV at the detector. The overall power loss through the lens system is approximately 9 dB at the optical axis. The spatial resolution of the SPC is approximated as 6.25 mm from the 5 cm aperture size and the pixel count. As an imaging target, an aluminum stencil hidden between two cardboard sheets was placed in the object plane. A picture of the SPC setup is shown in Fig. 17(b).

The modulation diversity available from the source SoC can be adopted for THz SPCs in a number of ways. Two different imaging methods are demonstrated here. In the first method, single pixel switching was used. A set of 64 illumination patterns representing an identity matrix were pre-loaded to the cache. Such sequence performs a raster scanning of the target one pixel at a time. The SoC was globally chopped at a frequency of 1 MHz to avoid 1/f noise from the detector. The 3-dB readout bandwidth of the detector output was 2 MHz. Thereafter, patterns were triggered using the FPGA and for each pattern, the fundamental 1 MHz signal tone received at the spectrum analyzer was filtered and recorded. As noted previously in Section III, this process can be repeated indefinitely over the circular FIFO cache without requiring another time-consuming memory load operation. A 100 ms acquisition time was observed for one 64-pixel image with a 60 dB voltage DR, resulting in a 10-fps imaging rate. An image sample is shown in Fig. 18(a). Here, the image acquisition time was primarily limited by the spectrum analyzer readout period.

For the second method, a full FDM scheme was used. Here, all the pixels were turned on simultaneously, and FDM hardware was used to chop each pixel at a different frequency. A 25 MHz CClk signal was supplied from the FPGA, and MFDs were programmed for frequency-division factors K in the range of 17 to 34. These were selected to place all chopping frequencies between the fundamental and second harmonics of the lowest component (0.73 MHz). Thereafter, a baseband spectrum covering all chopping frequencies was acquired at the spectrum analyzer. Individual pixels were located by means of a look-up table to render an image from a single spectrum. One such image and the corresponding baseband spectrum are shown in Fig. 18(b) and Fig. 18(c), respectively. With this technique, each image was captured in 40 ms, and a 25-fps video-rate imaging was demonstrated. Note that the readout of a wide baseband spectrum in a short period required a higher video bandwidth at the spectrum analyzer, which resulted in a reduced voltage DR of 40 dB as compared to the first method. These two examples denote the speed and SNR trade-off that can be present in a THz SPC. Depending on the baseband characteristics, the modulation diversity at the source SoC can be reconfigured to provide an optimal imaging performance. Due to the high SNR and high-speed pixel switching available from the SoC, the imaging rate can be extended to thousands of frames per second with an optimized baseband readout.

VII. Conclusion

In this paper, an 8×8 pixel, 0.42 THz source SoC has been presented that is specifically designed for versatile CTI applications. The key features of the SoC include fast and incoherent spatial light modulation that can be electronically multiplexed over different chopping rates, and in-situ power monitoring from each pixel through an integrated BIST. The chip architecture also allows potential board level integration of multiple SoCs for large size, high pixel count CTI apertures. While earlier THz SPC efforts have been focused on external

TABLE I
STATE-OF-THE-ART IN SILICON INTEGRATED THZ SOURCES

	This work	[13]	[12]	[17]	[36]	[11]	[37]	[38]	[18]
Technology	130nm SiGe BiCMOS	130nm SiGe	130nm SiGe	65nm bulk CMOS	45nm SOI CMOS	130nm SiGe	40nm bulk CMOS	40nm CMOS	65nm CMOS
Freq. (GHz)	420	530	317	338	420	1010	586.7	660.8–676.6	416
P_{rad} (dBm)	**10.3**	0	5.2	-0.9	-10	-10.9	0.1	-16.1	-3
Coherent	**No**	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
EIRP (dBm)	**31.21**†	25†	22.5	17.1	3	13.1	24.1	7.4	14
Radiators	64	16	16	16	8	91	36	8	16
Power/radiator (dBm)	**-3.54**$^{\perp}$	-11.3$^{\perp}$	-6.84$^{\#}$	-12.9$^{\#}$	-19.03$^{\#}$	-30.05$^{\#}$	-15.5$^{\perp}$	-25.13$^{\#}$	-15.04$^{\#}$
Tuning (%)	0.7	3.2	0.06	2.1	10	–	0.7	2.36§	1.7
Efficiency (%)	0.24*/0.17**	0.04	0.54	0.053	0.014	0.0073	0.08	0.02	0.034
Area (mm^2)	12.6	4.2	2.1	3.9	10.26	1	0.68	0.862	4.1
Mod. rate*	**10 MHz**‡	–							
FDM¶	**Yes**	No							
BIST¶	**Yes**	No							
SoC¶	**Yes**	No							

†Single pixel; $^{\perp}$Incoherent; $^{\#}$Net coherent output power normalized to number of radiators; §Estimated ;
¶Applicable only to incoherent arrays; *Peak efficiency; **At peak power; ‡3-dB power roll-off.

THz SLMs, this SoC presents a practical, all-electronic, compact, silicon-integrated THz SLM radiation source for the first time, that also provides dedicated FDM and BIST calibration for further CTI enhancements. A silicon only, 8×8 pixel THz SPC system is also demonstrated that is able to produce images at 25 fps with a DR of around 40 dB. With the use of appropriate baseband processing, a 10 MHz modulation rate available at the SoC can be used for ultra-fast THz imaging with thousands of frames per second.

A comparison of this work with other state-of-the-art (SoA) THz sources is presented in Table I. As noted, most of the existing research has focused on design of Si-integrated THz sources with coherent power combining [11], [12], [36], [38]. Coherent beam-steering arrays have also been reported in [17], [18], [37]. The limited EIRP of these sources can be problematic for design of sensitive imaging systems. Their scalability towards a higher radiation power is also limited because of the complexities associated with RF locking either mutually or with an external LO. Particularly, the coherent radiation can prove detrimental to the image fidelity in many situations due to the formation of interference speckles [15]. In contrast, this work shows that an incoherent THz source array can be advantageous in terms of scalability, output power, and illumination reconfigurability. This work extends the SoA incoherent THz power radiation from Si-integrated sources by a factor of 10.7 as compared to [13]. For 0.3 THz and above silicon integrated sources, the net incoherent power reported here is also more than 3 times higher than the best coherent power reported in [12]. The highest pixel EIRP of 31.21 dBm is also reported, that is achieved due to the combination of -3.54 dBm average power generated at each pixel with a 15 mm diameter lens. Another incoherent THz source array has been reported in [13] with 4×4 pixels. Compressive imaging using this source is also presented briefly in Section III-B of [6]. Compared to [13], this work extends the pixel resolution by a factor of 4 and integrates dedicated ASIC for high-speed, high SNR, and scalable THz imaging.

ACKNOWLEDGMENT

The authors would like to thank Dr. Bernd Heinemann from IHP Microelectronics, Frankfurt (oder), Germany; and R. Zatta, M. Andree, and W. Förster from the University of Wuppertal, Germany for their help.

REFERENCES

[1] D. Woolard, R. Brown, M. Pepper, and M. Kemp, "Terahertz frequency sensing and imaging: A time of reckoning future applications?" *Proceedings of the IEEE*, vol. 93, no. 10, pp. 1722–1743, Oct 2005. [Online]. Available: https://doi.org/10.1109/jproc.2005.853539

[2] I. Duling and D. Zimdars, "Revealing hidden defects," *Nature Photonics*, vol. 3, no. 11, pp. 630–632, Nov. 2009. [Online]. Available: https://doi.org/10.1038/nphoton.2009.206

[3] B. Ferguson and X.-C. Zhang, "Materials for terahertz science and technology," *Nature Materials*, vol. 1, no. 1, pp. 26–33, Sep 2002. [Online]. Available: https://doi.org/10.1038/nmat708

[4] J. A. Zeitler and Y.-C. Shen, "Industrial applications of terahertz imaging," in *Terahertz Spectroscopy and Imaging*. Springer Berlin Heidelberg, 2012, pp. 451–489.

[5] P. Hillger, R. Jain, J. Grzyb, W. Forster, B. Heinemann, G. MacGrogan, P. Mounaix, T. Zimmer, and U. R. Pfeiffer, "A 128-pixel system-on-a-chip for real-time super-resolution terahertz near-field imaging," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3599–3612, dec 2018. [Online]. Available: https://doi.org/10.1109/jssc.2018.2878817

[6] P. Hillger, J. Grzyb, R. Jain, and U. R. Pfeiffer, "Terahertz imaging and sensing applications with silicon-based technologies," *IEEE Transactions on Terahertz Science and Technology*, vol. 9, no. 1, pp. 1–19, Jan. 2019. [Online]. Available: https://doi.org/10.1109/tthz.2018.2884852

[7] D. Arnone, C. Ciesla, and M. Pepper, "Terahertz imaging comes into view," *Physics World*, vol. 13, no. 4, pp. 35–40, Apr 2000. [Online]. Available: https://doi.org/10.1088/2058-7058/13/4/24

[8] R. A. Hadi, H. Sherry, J. Grzyb, Y. Zhao, W. Forster, H. M. Keller, A. Cathelin, A. Kaiser, and U. R. Pfeiffer, "A 1 k-pixel video camera for 0.7–1.1 terahertz imaging applications in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2999–3012, Dec 2012. [Online]. Available: https://doi.org/10.1109/jssc.2012.2217851

[9] S. Yokoyama, M. Ikebe, Y. Kanazawa, T. Ikegami, P. Ambalathankandy, S. Hiramatsu, E. Sano, Y. Takida, and H. Minamide, "5.8 A 32x32-pixel 0.9THz imager with pixel-parallel 12b VCO-based ADC in 0.18μm CMOS," in *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*. IEEE, Feb 2019. [Online]. Available: https://doi.org/10.1109/isscc.2019.8662483

[10] J. Oden, J. Meilhan, J. Lalanne-Dera, J.-F. Roux, F. Garet, J.-L. Coutaz, and F. Simoens, "Imaging of broadband terahertz beams using an array of antenna-coupled microbolometers operating at room temperature," *Optics Express*, vol. 21, no. 4, p. 4817, Feb 2013. [Online]. Available: https://doi.org/10.1364/oe.21.004817

[11] Z. Hu, M. Kaynak, and R. Han, "High-power radiation at 1 THz in silicon: A fully scalable array using a multi-functional radiating mesh structure," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1313–1327, May 2018. [Online]. Available: https://doi.org/10.1109/jssc.2017.2786682

[12] R. Han, C. Jiang, A. Mostajeran, M. Emadi, H. Aghasi, H. Sherry, A. Cathelin, and E. Afshari, "A SiGe terahertz heterodyne imaging transmitter with 3.3 mW radiated power and fully-integrated phase-locked loop," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2935–2947, Dec 2015. [Online]. Available: https://doi.org/10.1109/jssc.2015.2471847

[13] U. R. Pfeiffer, Y. Zhao, J. Grzyb, R. A. Hadi, N. Sarmah, W. Forster, H. Rucker, and B. Heinemann, "A 0.53 THz reconfigurable source module with up to 1 mW radiated power for diffuse illumination in terahertz imaging applications," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2938–2950, Dec 2014. [Online]. Available: https://doi.org/10.1109/jssc.2014.2358570

[14] J. Grzyb, K. Statnikov, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 210–270-GHz circularly polarized FMCW radar with a single-lens-coupled SiGe HBT chip," *IEEE Transactions on Terahertz Science and Technology*, vol. 6, no. 6, pp. 771–783, Nov 2016. [Online]. Available: https://doi.org/10.1109/tthz.2016.2602539

[15] K. B. Cooper, R. J. Dengler, N. Llombart, B. Thomas, G. Chattopadhyay, and P. H. Siegel, "THz imaging radar for standoff personnel screening," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, no. 1, pp. 169–182, Sep 2011. [Online]. Available: https://doi.org/10.1109/tthz.2011.2159556

[16] D. M. Sheen, D. L. McMakin, and T. E. Hall, "Speckle in active millimeter-wave and terahertz imaging and spectroscopy," in *Passive Millimeter-Wave Imaging Technology X*, R. Appleby and D. A. Wikner, Eds. SPIE, Apr 2007. [Online]. Available: https://doi.org/10.1117/F12.721323

[17] Y. Tousi and E. Afshari, "14.6 A scalable THz 2D phased array with +17dBm of EIRP at 338GHz in 65nm bulk CMOS," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*. IEEE, Feb 2014. [Online]. Available: https://doi.org/10.1109/isscc.2014.6757425

[18] H. Saeidi, S. Venkatesh, C. R. Chappidi, T. Sharma, C. Zhu, and K. Sengupta, "29.9 A 4×4 distributed multi-layer oscillator network for harmonic injection and THz beamforming with 14dbm EIRP at 416GHz in a lensless 65nm CMOS IC," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*. IEEE, Feb 2020. [Online]. Available: https://doi.org/10.1109/isscc19947.2020.9063076

[19] M. F. Duarte, M. A. Davenport, D. Takhar, J. N. Laska, T. Sun, K. F. Kelly, and R. G. Baraniuk, "Single-pixel imaging via compressive sampling," *IEEE Signal Processing Magazine*, vol. 25, no. 2, pp. 83–91, Mar 2008. [Online]. Available: https://doi.org/10.1109/msp.2007.914730

[20] W. L. Chan, K. Charan, D. Takhar, K. F. Kelly, R. G. Baraniuk, and D. M. Mittleman, "A single-pixel terahertz imaging system based on compressed sensing," *Applied Physics Letters*, vol. 93, no. 12, p. 121105, Sep 2008. [Online]. Available: https://doi.org/10.1063/1.2989126

[21] C. M. Watts, D. Shrekenhamer, J. Montoya, G. Lipworth, J. Hunt, T. Sleasman, S. Krishna, D. R. Smith, and W. J. Padilla, "Terahertz compressive imaging with metamaterial spatial light modulators," *Nature Photonics*, vol. 8, no. 8, pp. 605–609, Jun 2014. [Online]. Available: https://doi.org/10.1038/nphoton.2014.139

[22] S. Rout and S. R. Sonkusale, "A low-voltage high-speed terahertz spatial light modulator using active metamaterial," *APL Photonics*, vol. 1, no. 8, p. 086102, Nov 2016. [Online]. Available: https://doi.org/10.1063/1.4958739

[23] M. Unlu, M. R. Hashemi, C. W. Berry, S. Li, S.-H. Yang, and M. Jarrahi, "Switchable scattering meta-surfaces for broadband terahertz modulation," *Scientific Reports*, vol. 4, no. 1, Jul 2014. [Online]. Available: https://doi.org/10.1038/srep05708

[24] S. Augustin, P. Jung, S. Frohmann, and H.-W. Hubers, "Terahertz dynamic aperture imaging at standoff distances using a compressed sensing protocol," *IEEE Transactions on Terahertz Science and Technology*, vol. 9, no. 4, pp. 364–372, Jul 2019. [Online]. Available: https://doi.org/10.1109/tthz.2019.2915640

[25] J. Xu and X.-C. Zhang, "Terahertz wave reciprocal imaging," *Applied Physics Letters*, vol. 88, no. 15, p. 151107, Apr 2006. [Online]. Available: https://doi.org/10.1063/1.2194822

[26] R. Jain, P. Hillger, J. Grzyb, and U. R. Pfeiffer, "29.1 A 0.42THz 9.2dBm 64-pixel source-array SoC with spatial modulation diversity for computational terahertz imaging," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*. IEEE, feb 2020. [Online]. Available: https://doi.org/10.1109/isscc19947.2020.9063025

[27] H. Caulfield, J. Kinser, and S. Rogers, "Optical neural networks," *Proceedings of the IEEE*, vol. 77, no. 10, pp. 1573–1583, 1989. [Online]. Available: https://doi.org/10.1109/5.40669

[28] K. K.O., W. Choi, Q. Zhong, N. Sharma, Y. Zhang, R. Han, Z. Ahmad, D.-Y. Kim, S. Kshattry, I. R. Medvedev, D. J. Lary, H.-J. Nam, P. Raskin, and I. Kim, "Opening terahertz for everyday applications," *IEEE Communications Magazine*, vol. 57, no. 8, pp. 70–76, aug 2019. [Online]. Available: https://doi.org/10.1109/mcom.2019.1800909

[29] P. Hillger, J. Grzyb, S. Malz, B. Heinemann, and U. Pfeiffer, "A lens-integrated 430 GHz SiGe HBT source with up to -6.3 dBm radiated power," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. IEEE, Jun 2017. [Online]. Available: https://doi.org/10.1109/rfic.2017.7969042

[30] J. Grzyb, H. Sherry, Y. Zhao, R. A. Hadi, A. Cathelin, A. Kaiser, and U. Pfeiffer, "Real-time video rate imaging with a 1k-pixel THz CMOS focal plane array," in *Passive and Active Millimeter-Wave Imaging XV*. SPIE, may 2012. [Online]. Available: https://doi.org/10.1117/12.919218

[31] D. Rutledge and M. Muha, "Imaging antenna arrays," *IEEE Transactions on Antennas and Propagation*, vol. 30, no. 4, pp. 535–540, jul 1982. [Online]. Available: https://doi.org/10.1109/tap.1982.1142856

[32] R. Jain, J. Grzyb, and U. R. Pfeiffer, "Terahertz light-field imaging," *IEEE Transactions on Terahertz Science and Technology*, pp. 1–9, 2016. [Online]. Available: https://doi.org/10.1109/tthz.2016.2584861

[33] M. Andree, J. Grzyb, R. Jain, B. Heinemann, and U. R. Pfeiffer, "A broadband dual-polarized terahertz direct detector in a 0.13-μm SiGe HBT technology," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*. IEEE, Jun 2019. [Online]. Available: https://doi.org/10.1109/mwsym.2019.8700871

[34] R. Zatta, R. Jain, and U. Pfeiffer, "Characterization of the noise behavior in lens-integrated CMOS terahertz video cameras," *Terahertz Sicience and Technology-The International Journal of THz*, vol. 11, no. 4, pp. 102–123, 2018. [Online]. Available: https://www.doi.org/10.11906/TST.102-123.2018.12.10

[35] D. Filipovic, G. Gauthier, S. Raman, and G. Rebeiz, "Off-axis properties of silicon and quartz dielectric lens antennas," *IEEE Transactions on Antennas and Propagation*, vol. 45, no. 5, pp. 760–766, may 1997. [Online]. Available: https://doi.org/10.1109/8.575618

[36] F. Golcuk, O. D. Gurbuz, and G. M. Rebeiz, "A 0.39–0.44 THz 2x4 amplifier-quadrupler array with peak EIRP of 3–4 dBm," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 12, pp. 4483–4491, Dec 2013. [Online]. Available: https://doi.org/10.1109/tmtt.2013.2287493

[37] K. Guo and P. Reynaert, "29.2 A 0.59THz beam-steerable coherent radiator array with 1mW radiated power and 24.1dBm EIRP in 40nm CMOS," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*. IEEE, Feb 2020. [Online]. Available: https://doi.org/10.1109/isscc19947.2020.9063139

[38] G. Guimaraes and P. Reynaert, "29.6 A 660-to-676GHz 4×2 oscillator-radiator array with intrinsic frequency-filtering feedback for harmonic power boost achieving 7.4dBm EIRP in 40nm CMOS," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*. IEEE, Feb 2020. [Online]. Available: https://doi.org/10.1109/isscc19947.2020.9063037

Ritesh Jain received his M.Tech degree in Electrical Engineering from the Indian Institute of Technology (IIT) Gandhinagar, Gujarat, India in 2014. In 2013-2014, he was a joint research fellow with the Technical University of Berlin and IHP Microelectronics, Frankfurt (Oder) in Germany where he was exploring process optimization techniques for CMOS THz power detectors. Since 2014, he has been pursuing a Ph.D. degree at the Institute for High-Frequency and Communication Technology (IHCT), University of Wuppertal, Germany. He is the recipient of President's Gold medal for the M.Tech program 2014 batch at IIT Gandhinagar, and the co-recipient of 2018 Jan Van Vessem Award for Outstanding European Paper at IEEE International Solid State Circuits Conference. His current research interests include silicon-integrated mmWave and THz imaging and sensing systems.

Philipp Hillger received his B.Sc. and M.Sc. degree in electrical engineering from the Ruhr-University Bochum, Germany, in 2011 and 2014, respectively. From 2011 to 2013, he was a working student at Intel Mobile Comminucations, Duisburg, Germany, where he was involved in IC design and system engineering for various wireless standards. In 2014 he joined the Institure for High-Frequency and Communication Technolgy (IHCT) in Wuppertal, Germany, where he received his Ph.D. in 2020. He is the recipient of the 2018 Jan Van Vessem Award for Outstanding European Paper. His major fields of intrest are silicon-based mmWave and THz systems for imaging, sensing and communication.

Eamal Ashna received the B.Sc. and M.Sc. degree electrical engineering degree specialized in Information Technology and Communications from the University of Wuppertal, Germany, in 2017 and 2020 respectively. He joined the Institute for High frequency and Communication Technology in 2020 and is currently working towards his Ph.D. degree. His research interests focuses on Computational THz Imaging systems with modern nanoscale CMOS and SiGe-HBT technology.

Janusz Grzyb received the M.Sc. degree (cum laude) in electronic engineering (with a major in the synthesis and design of analog CMOS and BiCMOS circuits with an individual study program from the Integrated Circuits Laboratory, Gdańsk University of Technology, Gdańsk, Poland, in 1998, and the Ph.D. degree from the Swiss Federal Institute of Technology Zurich, Switzerland, in 2004. In 1999, he joined the Electronics Labs, Swiss Federal Institute of Technology, where he performed pioneering work in the area of low-cost large-area panel processing multichip-module-based system in package solutions for 60-, 77-, and 94-GHz applications. He was a Research Assistant with the Gdańsk University of Technology from 1998 to 1999. From 2004 to 2006, he was with the Communication System Design and High-Speed/Optical Packaging Groups, IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, where he was involved in the development of the low-cost packaged highly integrated SiGe transceiver for 60-GHz Gb/s wireless data communication. From 2006 to 2009, he was with the Research and Development Group, Huber & Suhner, Pfäffikon ZH, Switzerland, where he brought onto the market one of the world's first commercially available point-to-point 60-GHz links: the Sensity Link System. Since 2009, he has been with the Institute for High-Frequency and Communication Technology University of Wuppertal, Wuppertal, Germany. His current research interests include all aspects of silicon-integrated terahertz electronics. Dr. Grzyb was a co-recipient of the 2006 Lewis Winner Award for Outstanding Paper of the IEEE International Solid-State Circuit Conference, the 2006 IBM Pat Goldberg Memorial Best Paper Award, the 2012 and 2018 Jan Van Vessem Award for Outstanding European Paper of the IEEE International Solid State Circuits Conference, and the 2014 Best Paper Award of the European Conference on Antennas and Propagation and the Microwave Prize 2017 of the IEEE Microwave Theory and Techniques Society.

Ullrich R. Pfeiffer (M02SM06F20) received the diploma degree in physics and the Ph.D. in physics from the University of Heidelberg, Germany, in 1996 and 1999 respectively. In 1997 he worked as a research fellow at the Rutherford Appleton Laboratory, Oxfordshire England. From 1999-2001 he was working as a Postdoctoral Researcher, at the University of Heidelberg on real-time electronics for particle physics experiments at the European Organization for Nuclear Research (CERN), Switzerland. From 2001 to 2006 he was with the IBM T.J. Watson Research Center where his research involved RF circuit design, power amplifier design at 60GHz and 77GHz, high-frequency modeling and packaging for millimeter-wave communication systems. In 2007 he received a European Young Investigator Award and lead the THz electronics group at the Institute of High-Frequency and Quantum Electronics at the University of Siegen, Germany. Since 2008 he holds the High-frequency and Communication Technology chair at the University of Wuppertal, Germany. His current research includes silicon RFICs for mmWave/THz communication, radar and imaging systems.

He was the co-recipient of the 2004 and 2006 Lewis Winner Award for Outstanding Paper at the IEEE International Solid-State Circuit Conference, the co-recipient of the 2006 IBM Pat Goldberg Memorial Best Paper Award, the 2008 EuMIC Best Paper Award, the 2010 EuMC Microwave Prize, the 2014 EuCAP Best Paper Award, and the 2017 Microwave Prize, the 2012 and 2018 Jan Van Vessem Award for Outstanding European Paper at the IEEE International Solid-State Circuit Conference. He has been a Distinguished Lecturer for the IEEE Solid-State Circuits Society and the president of the German Association for Electrical Engineering and Information Technology e.V. (FTEI).